STC5230-I

Synchronous Clock for SETS

Data Sheet

Description

The RoHS 6/6 compliant STC5230-I is a single chip solution for the timing source in SDH, SONET, and Synchronous Ethernet network elements. The device is fully compliant with ITU-T G.813, G.8262, Telcordia GR1244, and GR253.

The STC5230-I accepts 12 reference inputs and generates 9 independent synchronized output clocks. Reference inputs are individually monitored for activity and quality. Reference selection may be automatic, manual, and hard-wired manual. Active reference selection may be manual or automatic. All reference switches are hitless. Synchronized outputs may be programmed for some certain SONET and SDH as well as Synchronous Ethernet frequencies or wide variety of frequencies from 1MHz up to 156.25MHz, in 1kHz steps.

Two independent timing generators, T0 and T4, provide the essential functions for Synchronous Equipment Timing Source (SETS). Each timing generator includes a DPLL (Digital Phase-Locked Loop), which may operate in the Freerun, Synchronized, and Holdover modes. Timing generator T0 supports master/slave operation for redundant applications. The proprietary **SyncLink^{TM}** cross-couple data link provides master/slave phase information and state data to ensure seamless side switches.

A standard SPI serial bus interface provides access to the STC5230-I's comprehensive, yet simple to use internal control and status registers. The device operates with an external OCXO or TCXO.

The STC5230-I may be field upgraded with an optional external EEPROM or via the bus interface.

Features

- Suitable for SDH SETS, SONET Stratum 3, 4E, 4 and SMC, and Synchronous Ethernet
- Two timing generators, T0 and T4, for SETS
- Complies with ITU-T G.813 opt1/2, G.8262 EEC opt1/2, Telcordia GR1244 and GR253
- Supports Master/Slave for redundant application with the **SyncLink^{TM}** cross-couple data links
- Supports 4 different frequencies of external oscillator (programmable): 10MHz, 12.8MHz, 19.2MHz, 20MHz
- Accepts 12 individual clock reference inputs
- Supports automatically frequency detection or manually acceptable frequency. Each reference input is monitored for activity and quality
- Supports manual and automatic reference selection
- 9 synchronized output clocks
- T0 and T4 have independent reference lists and priority tables for automatic reference selection
- Provides compensation for the phase delay of the master/slave cross-couple links, in 0.1ns steps up to 409.5ns
- Provides measurement of the round-trip phase delay of the master/slave cross-couple links.
- Phase align locking and hit-less reference switching
- Phase rebuild on re-lock and reference switches
- Programmable loop bandwidth (T0/T4) 0.1Hz to 103Hz
- Supports SPI bus interface
- Field upgrade capability
- IEEE 1149.1 JTAG boundary scan
- Available in TQFP100 package

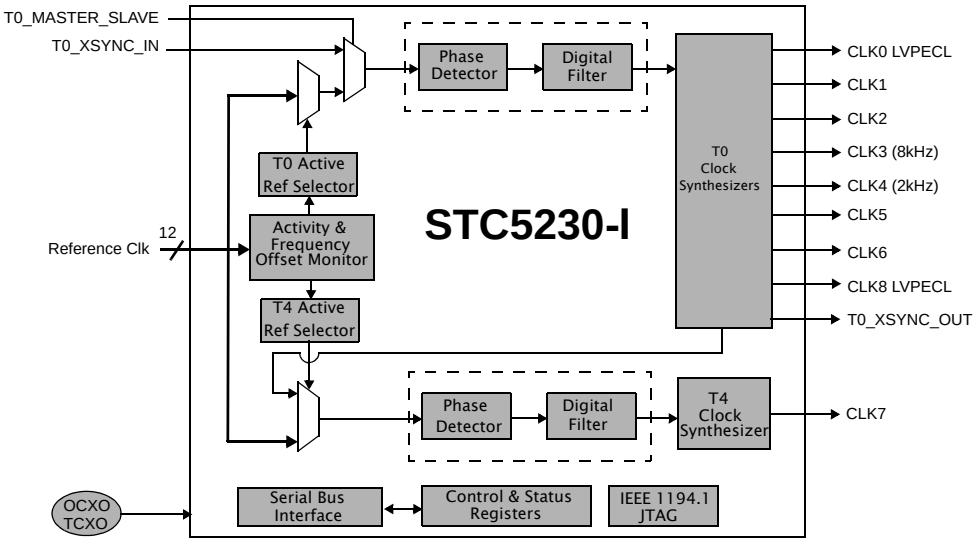
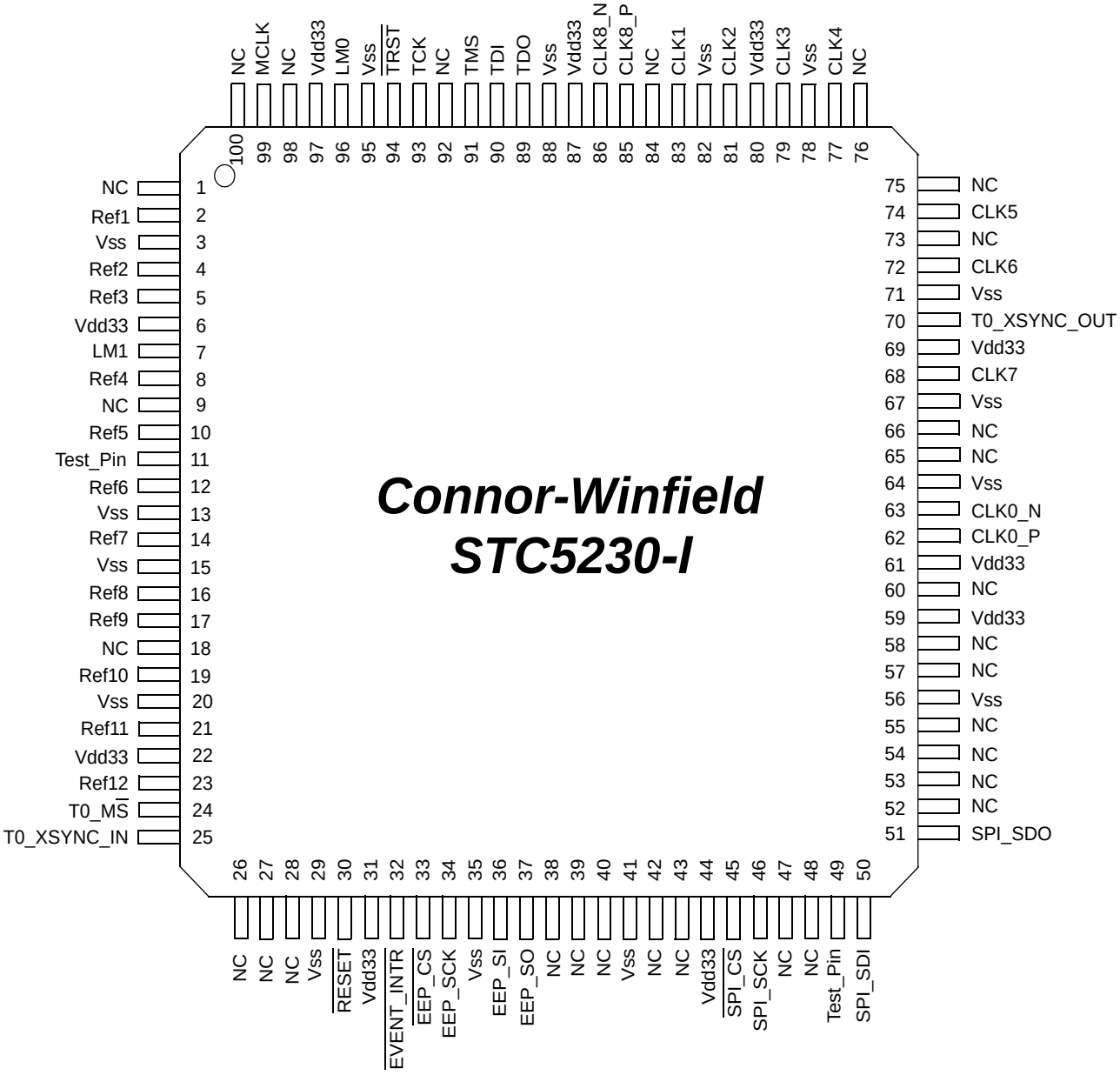


Figure 1: Functional Block Diagram

Table of Contents

Table of Figures

STC5230-I Pin Diagram (Top View)



Note: Pins labeled “Test Pin” must be grounded.

STC5230-I Pin Description

All I/O is LVCMOS, except for CLK0 and CLK8, which are LVPECL.

Table 1: Pin Description

Pin Name	Pin #	I/O	Description
Vdd33	6,22,31, 44,59,61, 69,80, 87,97		3.3V power input
Vss	3,13,15, 20,29,35, 41,56,64, 67,71,78, 82,88,95		Digital ground
$\overline{\text{TRST}}$	94	I	JTAG boundary scan reset, active low
TCK	93	I	JTAG boundary scan clock
TMS	91	I	JTAG boundary scan mode selection
TDI	90	I	JTAG boundary scan data input
TDO	89	O	JTAG boundary scan data output
$\overline{\text{RESET}}$	30	I	Active low to reset the chip
MCLK	99	I	Master clock input, 20 MHz
$\overline{\text{SPI\_CS}}$	45	I	SPI bus chip select ($\overline{\text{CS}}$)
SPI_SCK	46	I	SPI bus clock input (SCLK)
SPI_SDI	50	I	SPI bus data input (SDI)
SPI_SDO	51	O	SPI bus data output (SDO)
EEP_SO	37	I/O	Optional external EEPROM SO
EEP_SI	36	I/O	Optional external EEPROM SI
EEP_SCK	34	I/O	Optional external EEPROM SCK
$\overline{\text{EEP\_CS}}$	33	I/O	Optional external EEPROM $\overline{\text{CS}}$
$\overline{\text{EVENT\_INTR}}$	32	O	Event interrupt
REF1	2	I	Reference input 1
REF2	4	I	Reference input 2
REF3	5	I	Reference input 3
REF4	8	I	Reference input 4
REF5	10	I	Reference input 5
REF6	12	I	Reference input 6
REF7	14	I	Reference input 7
REF8	16	I	Reference input 8
REF9	17	I	Reference input 9
REF10	19	I	Reference input 10

Table 1: Pin Description

Pin Name	Pin #	I/O	Description
REF11	21	I	Reference input 11
REF12	23	I	Reference input 12
T0_M/$\overline{S}$	24	I	Select master or slave mode for T0, 1: Master, 0: Slave
T0_XSYNC_IN	25	I	Cross-couple **SyncLink™** data link input for T0 for master/slave redundant applications
T0_XSYNC_OUT	70	O	Cross-couple **SyncLink™** data link output for T0 for master/slave redundant applications
CLK0_P	62	O[1]	155.52/125 MHz LVPECL output (T0) or 1MHz to 156.25MHz, in 1kHz steps
CLK0_N	63	O[1]	155.52/125 MHz LVPECL output (T0) or 1MHz to 156.25MHz, in 1kHz steps
CLK1	83	O	19.44/38.88/51.84/77.76/25/50/125MHz (T0) or 1MHz to 156.25MHz, in 1kHz steps
CLK2	81	O	19.44/38.88/51.84/77.76/25/50/125MHz (T0) or 1MHz to 156.25MHz, in 1kHz steps
CLK3	79	O	8 kHz frame pulse or 50% duty cycle clock (T0)
CLK4	77	O	2 kHz frame pulse or 50% duty cycle clock (T0)
CLK5	74	O	44.736/34.368 MHz (T0) or 1MHz to 156.25MHz, in 1kHz steps
CLK6	72	O	1.544/3.088/6.176/12.352/24.704/2.048/4.098/8.192/16.384/32.768 MHz (T0) or 1MHz to 156.25MHz, in 1kHz steps
CLK7	68	O	1.544/2.048 MHz (T4) or 1MHz to 156.25MHz, in 1kHz steps
CLK8_P	85	O[1]	125 MHz LVPECL output (T0) or 1MHz to 156.25MHz, in 1kHz steps
CLK8_N	86	O[1]	125 MHz LVPECL output (T0) or 1MHz to 156.25MHz, in 1kHz steps
LM0	96	I	Hardware and firmware configuration data mode pin 0
LM1	7	I	Hardware and firmware configuration data mode pin 1
Test_Pin	11,49	I	Test pins, must be grounded for normal operation
NC	1, 9, 18, 26, 27, 28,38, 39,40,42, 43, 47, 48,52, 53, 54,55,57, 58, 60, 65, 66, 73, 75, 76, 84, 92, 98, 100		Pins may be connected to ground(0V) up to Vdd, or floating

Note 1: CLK0 and CLK8 are LVPECL

Absolute Maximum Ratings

Table 2: Absolute Maximum Ratings

Symbol	Parameter	Min.	Max	Units	Notes
Vdd33	Logic power supply voltage, 3.3V	-0.5	4.5	volts	2
VIN	Logic input voltage	-0.5	5.5	volts	2
TSTG	Storage Temperature	-65	150	°C	2

Note 2: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.

Operating Conditions and Electrical Characteristics

Table 3: Recommended Operating Conditions and Electrical Characteristics

Symbol	Parameter		Min.	Nominal	Max.	Units	Notes
Vdd33	3.3V digital power supply voltage		3.0	3.3	3.6	Volts	
CIN	Input capacitance			8		pF	
TRIP	Input reference signal positive pulse width		10			ns	
TRIN	Input reference signal negative pulse width		10			ns	
TJ	Operational Junction Temperature				125	°C	
TA	Operating Ambient Temperature Range (Commercial)		0		70	°C	
TA	Operating Ambient Temperature Range (Industrial)		-40		85	°C	
Icc (Vcc)	3.3V digital supply current			TBD		mA	
Icc (AVcc)	3.3V analog supply current			TBD		mA	
Pd	Device power dissipation			TBD		W	
VIH (3.3V)	LVCMOS	High level input voltage	2.0		5.5	Volts	3
VIL (3.3V)	LVCMOS	Low level input voltage	-0.3		0.8	Volts	3
VOH (3.3V)	LVCMOS	High level output voltage (IOH = -12mA)	2.4			Volts	3
VOL (3.3V)	LVCMOS	Low level output voltage (IOL =12mA)			0.4	Volts	3
V_T	LVCMOS	Threshold point	1.45	1.58	1.74	Volts	3
I_L	LVCMOS	Input Leakage Current	-10		10	uA	3
Voh	LVPECL	Output voltage high	Vdd33 - 1.11		Vdd33 - 0.67	Volts	4
Vol	LVPECL	Output voltage low	Vdd33 - 2.0		Vdd33 - 1.4	Volts	4
Vod	LVPECL	Output differential voltage	0.8		2.66	Volts	4

Note 3: LVCMOS 3.3 compatible
Note 4: 50 ohms termination to 1.3 (= Vdd33 - 2.0) volts

Register Map

Table 4: Register Map

Addr	Reg Name	Bits	Type	Description
0x00	Chip_ID	15-0	R	Chip ID, 0x5230
0x02	Chip_Rev	7-0	R	Chip revision number
0x03	Chip_Sub_Rev	7-0	R	Chip sub-revision number
0x04	T0_MS_Sts	0-0	R	Indicates master/slave state of T0 timing generator
0x05	T0_Slave_Phase_Adj	11-0	R/W	Adjust T0 slave phase from 0 ~ 409.5 ns in 0.1 ns steps
0x09	Fill_Obs_Window	3-0	R/W	Leaky bucket fill observation window, 1 ~ 16 ms
0x0a	Leak_Obs_Window	3-0	R/W	Leaky bucket leak observation window, 1 ~ 16 times the Fill_Obs_Window
0x0b	Bucket_Size	5-0	R/W	Leaky bucket size, 0 ~ 63
0x0c	Assert_Threshold	5-0	R/W	Leaky bucket alarm assert threshold, 1 ~ 63
0x0d	De_Assert_Threshold	5-0	R/W	Leaky bucket alarm de-assert threshold, 0 ~ 62
0x0e	Freerun_Cal	10-0	R/W	Freerun calibration, - 102.4 ~ + 102.3 ppm
0x10	Disqualification_Range	9-0	R/W	Reference disqualification range (pull-in range), 0 ~ 102.3 ppm
0x12	Qualification_Range	9-0	R/W	Reference qualification range, 0 ~ 102.3 ppm
0x14	Qualification_Timer	5-0	R/W	Reference qualification timer, 0 ~ 63 s
0x15	Ref_Index_Selector	3-0	R/W	Determines which reference data is shown in register Ref_Info. Determines which of reference input is selected for manually acceptable reference input frequency
0x16	Ref_Info	15-0	R	Frequency offset and frequency info of the reference selected by register Ref_Index_Selector
0x18	Refs_Activity	12-0	R	Reference and cross reference activity
0x1a	Refs_Qual	11-0	R	Reference 1 ~ 12 qualification
0x1c	T0_Control_Mode	5-0	R/W	OOP, Manual/Auto, Revertive, HO_Usage, Phase Align Mode
0x1d	T0_Bandwidth	4-0	R/W	Loop bandwidth selection for T0
0x1e	T0_Auto_Active_Ref	3-0	R	Indicates automatically selected reference
0x1f	T0_Manual_Active_Ref	3-0	R/W	Selects the active reference in manual mode
0x20	T0_Device_Holdover_History	31-0	R	Device Holdover History for T0 relative to MCLK
0x24	T0_Long_Term_Accu_History	31-0	R	Long term Accumulated History for T0 relative to MCLK
0x28	T0_Short_Term_Accu_History	31-0	R	Short term Accumulated History for T0 relative to MCLK
0x2c	T0_User_Accu_History	31-0	R/W	User Holdover data for T0 relative to MCLK
0x30	T0_History_Ramp	6-0	R/W	Controls T0 long term history and short term history accumulation bandwidth and the locking stage's frequency ramp control
0x31	T0_Priority_Table	47-0	R/W	REF1-12 selection priority for automatic mode (T0)
0x37	T0_PLL_Status	7-0	R	T0 PLL status SYNC, LOS, LOL, OOP, SAP, AHR, HHA
0x38	T0_Accu_Flush	0-0	W	Flush/reset the long-term and the device holdover history for T0
0x39	T4_Control_Mode	5-0	R/W	OOP, Manual/Auto, Revertive, HO_Usage, Phase Align Mode
0x3a	T4_Bandwidth	4-0	R/W	Loop bandwidth selection for T4
0x3b	T4_Auto_Active_Ref	3-0	R	Indicates automatically selected reference
0x3c	T4_Manual_Active_Ref	3-0	R/W	Selects the active reference in manual mode
0x3d	T4_Device_Holdover_History	31-0	R	Device holdover history for T4 relative to MCLK
0x41	T4_Long_Term_Accu_History	31-0	R	Long term accumulated history for T4 relative to MCLK
0x45	T4_Short_Term_Accu_History	31-0	R	Short term accumulated history for T4 relative to MCLK
0x49	T4_User_Accu_History	31-0	R/W	User programmed holdover history for T4 relative to MCLK

Table 4: Register Map

Addr	Reg Name	Bits	Type	Description
0x4d	T4_History_Ramp	6-0	R/W	Controls T4 long term history and short term history accumulation bandwidth and the locking stage's frequency ramp control
0x4e	T4_Priority_Table	47-0	R/W	REF1-12 selection priority for automatic mode (T4)
0x54	T4_PLL_Status	7-0	R	T4 PLL status SYNC, LOS, LOL, OOP, SAP, AHR, HHA
0x55	T4_Accu_Flush	0-0	W	Flush/reset the long-term and the device holdover history for T4
0x56	CLK0_Sel	1-0	R/W	155.52/125 MHz or tri-state for CLK0 (Freq Pre Defined mode)
0x57	CLK1_Sel	2-0	R/W	19.44/38.88/51.84/77.76/25/50/125MHz or tri-state select for CLK1 (Freq Pre Defined mode)
0x58	CLK2_Sel	2-0	R/W	19.44/38.88/51.84/77.76/25/50/125 MHz or tri-state select for CLK2 (Freq Pre Defined mode)
0x59	CLK3_Sel	5-0	R/W	8kHz output 50% duty cycle or pulse width selection for CLK3
0x5a	CLK4_Sel	5-0	R/W	2kHz output 50% duty cycle or pulse width selection for CLK4
0x5b	CLK5_Sel	1-0	R/W	DS3/E3 select for CLK5 (Freq Pre Defined mode)
0x5c	CLK6_Sel	3-0	R/W	DS1 x n / E1 x n select for CLK6 (Freq Pre Defined mode)
0x5d	CLK7_Sel	1-0	R/W	DS1/E1 select for CLK7 (Freq Pre Defined mode)
0x5e	Intr_Event	8-9,5-0	R/W	Interrupt event
0x60	Intr_Enable	8-9,5-0	R/W	Interrupt enable
0x62	T0_MS_PHE	19-0	R	Round-trip phase delay of T0's cross-couple data links
0x65	CLK8_Sel	1-0	R/W	125 MHz clock enable or disable for CLK8 (Freq Pre Defined mode)
0x66	CLK_Index_Select	2-0	R/W	Determine which clock output is selected to program frequency in Freq User Defined mode or adjust phase skew for clock output.
0x67	CLK_User_Defined_Freq	17-0	R/W	Enable Freq Pre Defined mode or select clock output frequency in Freq User Defined mode for CLK0~CLK8 (except CLK3 and CLK4)
0x68				
0x69				
0x6a	CLK_Skew_Adj	11-0	R/W	Adjust phase skew for CLK0~CLK8 and T0_XSYNC_OUT
0x6b				
0x6c	Manual_Accept_Ref_Freq	14-0	R/W	Select integer N for manually acceptable frequency at Nx8kHz; Enable auto detection of reference input frequency
0x6d				
0x7F	MCLK_Freq_Reset	7-0	R	Select the frequency of the external oscillator

Extra Registers if **Configuration Data Mode** is set as ***ROM_MODE***				
0x75	ROM_Loader_Status	2-0	R	Checksum status of core, hardware and firmware configuration data

Extra Registers if **Configuration Data Mode** is set as ***BUS_MODE***				
0x70	Bus_Loader_Status	2-0	R	Loading status of the hardware and firmware configuration data
0x71	Bus_Loader_Data	7-0	W	Data port of the bus loader of the hardware and firmware configuration data
0x72	Bus_Loader_Counter	13-0	R	Data counter of the bus loader of the hardware and firmware configuration data
0x75	Bus_Core_Status	0-0	R	Checksum status of core configuration data

Extra Registers if **Configuration Data Mode** is set as ***EEP_MODE***				
0x70	EEP_Loader_Checksum	0-0	R	Checksum status of the EEPROM loader of the hardware and firmware configuration data
0x71	EEP_Controller_Mode	7, 0	R/W	Mode of the EEPROM controller
0x72	EEP_Controller_Cmd	1-0	W	Command for the EEPROM controller

0x73	EEP_Controller_Page	7-0	W	Page number for the EEPROM controller
0x74	EEP_Controller_Data	7-0	R/W	Data port of the EEPROM controller
0x75	EEP_Core_Status	0-0	R	Checksum status of core configuration data

Master Clock Frequency

The STC5230-I supports four different frequencies of master clock: 10MHz, 12.8MHz, 19.2MHz, and 20MHz. See Chip Master Clock for details. Initial default accepted frequency of MCLK is 20MHz.

Table 5: Master Clock Frequency

12.8MHz
10MHz
19.2MHz
20MHz (Initial default frequency)

Input and Output Frequencies

Input Frequencies

Auto-Detect Acceptable Input Frequencies

The STC5230-I can automatically detect the frequency of the reference input when the user enable the auto-detection function for Ref1~Ref12 individually at the registers **Ref_Index_Selector** and **Manual Accept Ref Freq**. The acceptable frequency for auto detection is shown in Table 6

Table 6: Auto-Detect Acceptable Ref Input Frequencies

Reference Input	Frequency
REF1 ~ REF 12	8 kHz
	64 kHz
	19.44 MHz
	38.88 MHz
	77.76 MHz
	1.544 MHz
	2.048 MHz
	6.48 MHz
	8.192 MHz
	16.384 MHz
	25 MHz
	50 MHz
	125 MHz

Manually Acceptable Input Frequencies

STC5230-I provides another option which allows the user to select the manually acceptable reference frequency for all the reference inputs, at the integer multiple of 8kHz (Nx8kHz, N is integer from 1 to 32767). Hence the manually acceptable reference frequency range is 8kHz to 262.136MHz, in 8kHz steps. When a manually acceptable reference frequency is used, the user need to access the register **Ref Index Selector** and **Manual Accept Ref Freq**.

Input Frequency = N x 8kHz, where N = 1~32767

General Description

The STC5230-I is an integrated single chip solution for the synchronous clock in SDH (SETS), SONET, and Synchronous Ethernet network elements. Its highly integrated design implements all of the necessary ref-erence selection, monitoring, filtering, synthesis, and control functions. An external OCXO or TCXO com-pletes a system level solution (see Functional Block Diagram, Figure 1). The device supports four pro-grammable different frequencies of master clock: 10MHz, 12.8MHz, 19.2MHz, and 20MHz. Initial default accepted frequency is 20MHz.

The STC5230-I includes two timing generators, T0 and T4, to implement the essential ***Synchronous Equip-ment Timing Source*** (SETS) functions. Each timing generator may be in either external-timing or self-tim-ing mode. In external timing mode, a timing generator may individually select one of the external reference inputs as its active reference of its individual Digital Phase-Locked Loop (DPLL). In self-timing mode, the clock outputs are synthesized from the local oscillator (the external TCXO/OCXO). T0 provides 8 of the chip's 9 clock outputs while T4 provides one clock output. Additionally, T0 provides a cross reference output for master/slave applications.

Each timing generator can individually operate in ***Freerun***, ***Synchronized***, and ***Holdover*** mode. In synchronized mode, the DPLL phase-locks to the selected external reference. Phase lock may be set as arbitrary or zero phase offset between the active reference and clock outputs. Each DPLL's loop band-width may be programmed individually to vary the DPLL's filtering function. Conversely, both freerun and holdover modes are self-timing. In freerun mode, the clock outputs are synthesized and calibrated from the local oscillator. In holdover mode, the clock outputs are synthesized with a given frequency offset. This frequency offset may be either a frequency history previously accumulated by STC5230-I, or a user supplied frequency offset. The stability of freerun and holdover is simply determined by the local oscil-lator.

Each of reference inputs may be selected to accept either the auto-detect acceptable reference frequency or manually acceptable reference frequency. Each reference input is continuously monitored for activity and frequency offset. The activity monitoring is implemented with a leaky bucket accumulator reference is designated as "qualified" if it is active and its frequency offset is within the programmed range for a pre-programmed time.

Active references may be selected manually or automatically, individually selectable for T0 and T4. In manual mode, the active reference is selected under application control, independent of it's qualification status.

In automatic mode, the active reference is selected according to revertivity status, and each reference's priority and qualification. Reference priorities are individually programmable. T0 and T4 each have their own priority tables. Revertivity determines whether a higher priority qualified reference should preempt a qualified current active reference.

All reference switches are performed in a hitless manner. When references are switched, the device will minimize phase transitions in the output clocks. A frequency ramp control feature also ensures smooth frequency transitions into/out of both freerun and holdover mode.

STC5230-I provides two modes to program the frequency of CLK0~CLK8 (except CLK3 and CLK4) individually: Freq Pre Defined mode (default mode) and Freq User Defined mode. Phase skew of CLK0~CLK8 and T0_XSYNC_OUT is programmable.

Timing generator T0 supports master/slave operation for ***redundant applications***. T0 sends both the phase and reference selection information to the other T0 of the paired STC5230-Is via the proprietary SyncLink™ cross-coupled data link. The STC5230 may determine and report the T0 round-trip phase delay of the cross-couple data links.

The phase of the slave's clock outputs may be adjusted in 0.1ns step to compensate for the propa-gation and re-transmission delay of the cross-couple path. This will then minimize the phase hits to the downstream devices resulting from master/slave switches.

A serial bus interface (SPI) provides application access to the STC5230-I's internal control and status registers.

The STC5230-I also supports ***Field Upgradability***. The initialization of registers and PLL detailed behav-ior is defined by the hardware and firmware configu-ration data. This configuration data may be provided by the internal ROM or externally. When externally sourced, the data may be pumped either over the bus interface, or from an optional external EEPROM.

Detailed Description

Chip Master Clock

The device operates with an external oscillator (e.g., OCXO or TCXO) as its master clock, connected to the MCLK input, pin 99. Generally, user should select an oscillator has great stability and low phase noise as the master clock (MCLK).

The STC5230-I supports four different accepted fre-quencies of master clock: 10MHz, 12.8MHz, 19.2MHz, and 20MHz. Initial default accepted fre-quency of MCLK for STC5230 is 20MHz. When 10MHz, 19.2MHz, or 20MHz is selected as the fre-quency of MCLK, the user must write register **MCLK Freq Reset** three times consecutively, with no inter-vening read/writes from/ to other register. An internal soft-reset will occur after three writes completed. The accepted frequency of MCLK input returns to 20MHz following any regular reset. See register **MCLK Freq Reset** for details.

In the meantime, the STC5230-I allows user to read three values at the register **MCLK Freq Reset**: FRQID, COUNT, and ID Written Value.

FRQID
Indicates the ID of the frequency of MCLK that the STC5230 currently accept.

COUNT
Indicates how many times the register **MCLK Freq Reset** has been written to.

ID Written Value
Indicates the ID of associated value that is being writ-ten to the register **MCLK Freq Reset**.

See the register **MCLK Freq Reset** for more details.

Freerun Clock

The STC5230-I has an internal freerun clock synthe-sized from the MCLK. The frequency offset of the internal freerun clock can be calibrated by writing to the register Freerun Cali. It has the stability of the external TCXO/OCXO. The calibration offset may be programmed in 0.1ppm steps from -102.4 to +102.3ppm, in 2's complement.
This feature allow the user can digitally calibrate the freerun clock without physically adjusting the local oscillator.

Operating Mode General Description

The STC5230-I includes both a T0 and T4 timing gen-erators. Each timing generator has its own DPLL.

In general, each timing generator may individually be either in external-timing or self-timing mode. In exter-nal-timing mode, a timing generator may select any of the external references as the active reference for the DPLL. The active reference can be either one of the 12 input reference clocks, or the reference from the **T0_XSYNC_IN** cross-coupled links in slave mode, when devices are operated as master/slave pairs. In addition, T4 may select the output of T0 as its active reference. In self-timing mode, the clock outputs are synthesized from the MCLK (the external TCXO/ OCXO) (with a programmable calibration) or a given frequency offset.

In master mode, the timing generators may each operate in **Freerun**, **Synchronized**, or **Holdover** mode. Operating T0 timing generator in the slave mode is analogous to the synchronized/master. Both are in external-timing mode. In synchronized/master mode, the phase relationship between the reference and the clock outputs may be configured as arbitrary or aligned. The user may also program the DPLL's loop bandwidth to vary the noise transfer function. In slave mode, the clock outputs phase-align to the cross-reference, and the loop bandwidth is fixed (103 Hz).

Holdover mode is analogous to the freerun mode. Both are self-timing modes. The clock outputs are synthesized from the local oscillator with a program-mable calibration or a given frequency offset. The sta-bility in these two modes is simply determined by the local oscillator.

Operating Mode Details

The STC5230-I is designed to provide phase and fre-quency hit-less clock outputs to downstream devices, even through operating mode change and reference switches. Both the phase and frequency transitions will be continuous. The transfer into the self-timing mode (freerun and holdover) is designed to be fre-quency bump-less. A frequency ramp control limits the rate of frequency change through operating mode

change and reference switches. An application programmable maximum slew rate of 1, 1.5, and 2 ppm/second (or no slew rate limit) may be enforced, as written to the **T(0/4) History Ramp** registers.

Freerun/Master Mode

The **CLK(0-6,8)** (**CLK7** for T4) clock outputs are synthesized and may be calibrated from MCLK and have the stability of the external TCXO/OCXO. The calibration offset may be programmed by the application by writing to the **Freerun Cal** register. The calibration offset may be programmed from -102.4 to +102.3 ppm, in 0.1ppm steps.

Holdover/Master Mode

Holdover Mode is analogous to the freerun mode. The **CLK(0-6,8)** (**CLK7** for T4) clock outputs are synthesized from MCLK with a frequency offset, which is centered on the digitally calibrated freerun clock. The clock outputs will have the stability of the external TCXO/OCXO. The application may select the source of the frequency offset from either a device accumulated holdover history or a user supplied frequency offset by writing the "HO_Usage" bit of the **T(0/4) Control Mode** register. If the bit is set to **Device Accumulated History Holdover Mode**, the DPLL will use the device accumulated device holdover history to synthesize the clock outputs. If the bit is set to **User Supplied History Mode**, the DPLL outputs are synthesized according to an application supplied frequency offset, as provided in the **T(0/4) User Accu History** registers. To facilitate the user's accumulation of a holdover history, the user may read the short-term history of the current clock outputs from the **T(0/4) Short Term Accu History** register.

Synchronized/Master Mode

T0 timing generator is put into the Master mode by bringing the **T0_M/S** pin high. T4 timing generator only works in Master mode. In synchronized mode, the DPLL phase-locks and tracks to the selected input reference. The timing generator is in external-timing mode. The **CLK(0-6,8)** (**CLK7** for T4) clock outputs are all synchronized to the selected input reference.

In this mode, the "**Phase Align Mode**" bit of the **T(0/4) Control Mode** registers determines the output clock to input reference phase alignment mode. If both the bit is set to "**Align**" and frequency of the active reference is 8kHz, this timing generator runs in *align* mode, otherwise, it run in *arbitrary* mode. Running in arbitrary mode, the DPLL will initially operate in frequency locking mode in pull-in process. When the frequency of the reference is determined and locked, the clock output phase relationship relative to the reference input will be rebuild and locked. If running in align mode, the output clocks are phase aligned to the selected reference. (It should be noted that output-to-reference phase alignment is meaningful only in those cases where the output frequency and reference are the same or related by an integer ratio.)

After a reference switch or re-lock (due to loss of signal or loss of lock), the DPLL will be in a pull-in process initially. If the phase mode is set to be "arbitrary", the pull-in process will be frequency-locking only until the frequencies of the reference and output meet. Then, the clock output phase relationship relative to the reference input will be rebuild and locked. If the phase mode is set to be aligned, the pull-in process will be in phase-locking mode since the beginning. The pull-in process may prologue to 60+ seconds in normal situation.

Each DPLL's loop bandwidth may be set independently. Loop bandwidth is programmable from 100mHz to 103Hz by writing to the **T(0/4) Bandwidth** registers.

There are two special cases of the synchronized mode: **(a) Zombie mode** - If the signal of the active reference is lost, the DPLL output is generated according to the short-term history; and **(b) Out of Pull-in Range mode** - If the selected reference exceeds the pull-in range as programmed by the application, the DPLL output may be programmed to stay at the pull-in range limit, or to follow the reference. This is programmed by writing the "OOP" bit of the **T(0/4) Control Mode** registers, specifying whether to follow or not follow a reference that has exceeded the pull-in range. The frequency offset is relative to the digitally calibrated freerun clock.

Slave Mode

The slave mode is analogous to the synchronized/master mode. T0 timing generator will enter this mode by bringing the **T0_M/S** pin low. T4 timing generator does not support slave mode. Different from the synchronized/master mode, the phase of the output clock is aligned to the input cross-couple reference, not arbitrary. The loop bandwidth is fixed to 103 Hz. The DPLL's clock outputs will follow the cross-ref-

erence independent of the "OOP" bit of the **T0 Control Mode** registers. The DPLL will lock and phase align on the **T0_XSYNC_IN** input.

Operating Mode Transition Details

When the reference selection is set to manual mode, the operating mode is selected by writing to the **T(0/4) Manual Active Ref** registers. This forces the timing generator into freerun, synchronized, or holdover mode.

When the reference selection is set to automatic mode, the automatic reference selector picks the active reference and decides the operating mode. The DPLL will enter synchronized mode if at least one reference is qualified and selected as the active reference. Otherwise, the operating mode will be either freerun mode or holdover mode, depending on the availability of the holdover history.

Figure 2 shows the phase locked loop states and transitions for operation with automatic reference selection in Master mode. The transfer into and out of holdover mode is designed to be smooth and free of hits with frequency ramp control.

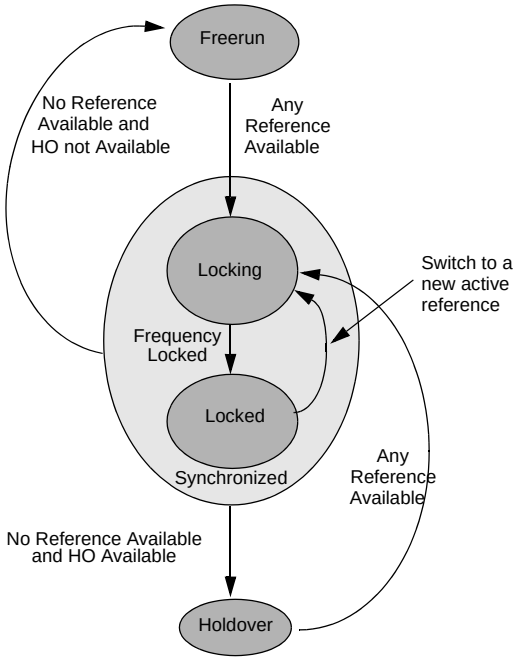


Figure 2: Operating mode transition in automatic reference selection (Master mode)

On all transitions into freerun or back from freerun, an application programmable maximum slew rate of 1, 1.5, or 2 ppm/second (or no slew rate limit) is applied, as written to the **T(0/4) History Ramp** registers.

History Accumulation Details

Three holdover histories are built and maintained by each timing generator: the **short-term history**, the **long-term history**, and the **device holdover history**.

1. Short-Term History
This is a short-term average frequency of the DPLL's clock outputs. The weighted 3rd order low-pass filter may be programmed for a -3dB point of 1.3 Hz, 0.64 Hz, 0.32 Hz, and 0.16 Hz by writing to the **T(0/4) History Ramp** register. The short-term history is used in the zombie sub-mode. This history may be read from the **T(0/4) Short Term Accu History** registers.

2. Long-Term History
This is a long-term average frequency of the DPLL's clock outputs, while synchronized to a selected external reference. The weighted 3rd order low-pass filter may be programmed for a -3dB point of 4.9 mHz, 2.5 mHz, 1.2 mHz, 0.62 mHz, 0.31 mHz, and 0.15 mHz by writing to the **T(0/4) History Ramp** register. Internally, an express mode is used after reset by applying a lower time constant for the first 15 minutes to speed up the history accumulation process. This accumulation process will be reset whenever the selected reference is switched or loss of lock occurs. The accumulation process will then resume after synchronization is achieved, as indicated by the assertion of "SYNC" bit in the **T(0/4) DPLL Status** register. Additionally, the application may flush/rebuild this long-term history by writing either "0" or "1" to the **T(0/4) Accu Flush** register. The long-term history may be read from the **T(0/4) Long Term Accu History** registers.

3. Device Holdover History
When the timing generator enters the holdover mode with the history usage programmed as Device Accumulated History Holdover Mode, this history determines the **CLK(0-6,8)** (**CLK7** for T4) clock outputs. The initial history will begin and be continuously updated by the long-term history after the completion of the 15 minute express mode time. Updating will stop if the long term history accumulation process is reset as a result of a reference switch or loss of lock. Thus, the previous holdover history will persist until a

new long term history is accumulated following a reference switch or the attendant re-building of the long term history after loss of lock. The “AHR” bit of the **T(0/4) DPLL Status** registers is set to “1” during updating, but will revert to “0” when updating stops. Additionally, the application may reset this holdover history by writing “1” to the **T(0/4) Accu Flush** register.

Phase-Locked Loop Status Details

The **T(0/4) PLL Status** registers contain the detailed status of the DPLLs, including the signal activity of the active reference, the synchronization status, and the availability of the holdover histories.

Applications can program the **Intr Enable** register to enable/disable the interrupts (pin **EVENT_INTR**) trigged by the status change of the **T(0/4) PLL Status** registers.

SYNC bit
In external-timing mode (e.g., slave and synchronized/master modes), this bit indicates the achievement of synchronization. This bit will not be asserted in self-timing mode (e.g., freerun and holdover modes).

LOS bit
In external-timing mode (e.g., slave and synchronized/master modes), this bit indicates the loss of signal on the active reference. This bit will not be asserted in self-timing mode (e.g., freerun and holdover modes).

LOL bit
In external-timing mode (e.g., slave and synchronized/master modes), the DPLL will set this bit if it fails to achieve or maintain lock to the active reference. This bit will not be asserted in self-timing mode (e.g., freerun and holdover modes). This bit is also not complementary to the SYNC bit. Both bits will not be asserted when the DPLL is in the pull-in process.

OOP bit
This bit indicates that the active reference is out of the pull-in range. This is meaningful only if in external-timing mode (e.g., slave and synchronized/master modes). This bit will not be asserted in self-timing mode (e.g., freerun and holdover modes). The frequency offset is relative to the digitally calibrated freerun clock.

SAP bit

This bit when set indicates that the DPLL’s output clocks have stopped following the active reference because the frequency offset of the active reference is out of pull-in range. The application can write to the **T(0/4) Control Mode** register to program whether the DPLL shall follow the active reference outside of the specified pull-in range.

AHR bit
This bit indicates whether the device holdover history is tracking on the current active reference (updating by the long-term history).

HHA bit
This bit indicates the availability of the holdover history, which may be either the user provided history or the device holdover history.

Reference Inputs Details

The STC5230 accepts 12 external reference inputs. The reference inputs may be selected to accept either the auto-detect acceptable reference frequency which can be automatically detected by STC5230 or manually acceptable reference frequency. All 12 reference inputs are monitored continuously for frequency, activity and quality. Each timing generator may select any of the reference inputs when the device is in external timing mode. T4 may accept T0’s output as its input via internal feedback path.

Acceptable Frequency and Frequency Offset Detection
The STC5230-I can automatically detect the frequency of the reference input when the user enable the auto-detection function for Ref1~Ref12 individually at the register **Ref Index Selector** and **Manual Accept Ref Freq**. The acceptable auto-detect frequencies are: 8kHz, 64kHz, 1.544MHz, 2.048MHz, 19.44MHz, 38.88MHz, 77.76MHz, 6.48MHz, 8.192MHz, 16.384MHz, 25MHz, 50MHz or 125MHz. These fre-quencies can be automatic detected continuously in the detector. Any carrier frequency change will be detected within 1ms. Each input is also monitored for frequency offset between input and the internal fre-erun clock. The frequency offset is a key factor to determine qualification of the reference inputs. See register **Ref Index Selector** and **Ref Info**.

STC5230 provides another option which allows the

user to select the manually acceptable reference frequency for all the reference inputs, at the integer mul-tiple of 8kHz (Nx8kHz, N is integer from 1 to 32767). Hence the manually acceptable reference frequency range is integer multiple of 8kHz from 8kHz to 262.136MHz. When a manually acceptable reference frequency is used, the user need to access the regis-ter **Ref Index Selector** and **Manual Accept Ref Freq**. Each input is monitored for frequency offset between input and the internal freerun clock. The fre-quency offset is shown in the register **Ref Info** when associate reference index is selected at the register **Ref Index Selector**.

Activity Monitoring

Activity monitoring is also a continuous process which is used to identify if the reference input is in normal. It is accomplished with a leaky bucket accumulation algorithm, as shown in Figure 3. The "leaky bucket" accumulator has a fill observation window that may be set from 1 to 16ms, where any hit of signal abnor-mality (or multiple hits) during the window increments the bucket count by one. The leak observation win-dow is 1 to 16 times the fill observation window. The leaky bucket accumulator decrements by one for each leak observation window that passes with no signal abnormality. Both windows operate in a con-secutive, non-overlapping manner. The bucket accu-mulator has alarm assert and alarm de-assert thresholds that can each be programmed from 1 to 64.

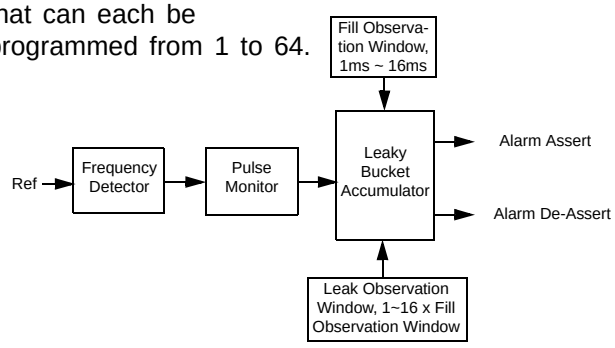


Figure 3: Activity Monitor

Applications can write to the following registers to configure the activity monitor: **Fill Obs Window**, **Leak Obs Window**, **Bucket Size**, **Assert Threshold**, and **De Assert Threshold**.

The user can set the bucket size equal to 0 to turn off the activity monitor. This de-asserts the activity alarms of all the references. Otherwise, a non-zero bucket size must be greater than or equal to the alarm assert threshold value, and the alarm assert threshold value must be greater than the alarm de-assert value. Attempted writes of invalid values will be ignored. Therefore, the user, when re-configuring the activity monitor, must carefully plan an appropriate sequence of writes.

Alarms appear in the **Refs Activity** register. A "1" indicates activity, and a "0" indicates an alarm, no activity. Note that if a reference is detected as a different frequency, the leaky bucket accumulator is set to the bucket size value and the reference will become inactive immediately.

Input Qualification

A reference qualification range may be programmed up to 102.3 ppm by writing to register **Qualification Range**, and a disqualification range set up to 102.3 ppm, by writing to register **Disqualification Range**. The qualification range must be set less than the disqualification range. Additionally, a qualification timer may be programmed from 0 to 63 seconds by writing to register **Qualification Timer**. The pull-in range is the same as the disqualification range.

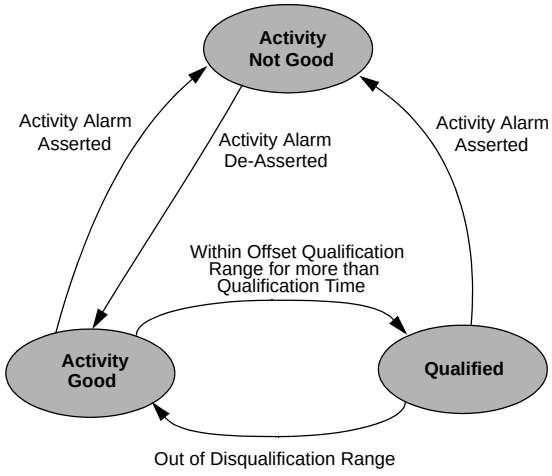


Figure 4: Reference Qualification Scheme

The frequency offset of each reference is relative to the digitally calibrated freerun clock may be read by selecting the reference in the **Ref_Selector** register and then reading the offset value from register **Ref Frq Offset**.

Figure 4 shows the reference qualification scheme. A

reference is qualified if it has no activity alarm and is within the qualification range for more than the qualification time. An activity alarm or frequency offset beyond the disqualification range will disqualify the reference. It may then be re-qualified if the activity alarm is off and the reference is within the qualification range for more than the qualification time.
The reference qualification status of each reference may then be read from register **Refs Qual**.

Active Reference Selection

The T0 and T4 timing generators may be individually operated in either manual or automatic input reference selection mode. The mode is selected via the **T(0/4) Control Mode** registers.

Manual Reference Selection Mode

In manual reference selection mode, the user may select the reference. This mode is selected via the **T(0/4) Control Mode** registers. The reference is selected by writing to the **T(0/4) Manual Active Ref** registers.

Automatic Reference Selection Mode

In automatic reference selection mode, the device will select one pre-qualified reference as the active reference. This mode is set via the **T(0/4) Control Mode** registers.

The active reference is picked according to its indicated priority in the reference priority table, registers **T(0/4) Priority Table**. Each reference has one entry in the table, which may be set to a value from 0 to 15. '0' masks-out the reference, while 1 to 15 set the priority, where '1' has the highest, and '15' has the lowest priority. The highest priority pre-qualified reference then is a candidate to be the active reference. If multiple references share the same priority, the one that has been qualified for the longest time will be selected.

The active reference candidate will be promoted to be the active reference immediately if no active reference exists. The operating mode will then enter synchronized mode.

If the candidate reference is not the existing active reference, it may or may not revert and pre-empt the existing active reference. This is determined by either enabling or disabling the "revertive" bit of the **T(0/4)_Control_Mode** to "1" for revertive or to "0" for non-revertive operation.

When reversion (pre-emption) is enabled, the candidate reference will be selected immediately as the new active reference. When reversion is disabled, the current active reference will not be pre-empted by any candidate until it is disqualified.

The automatically selected active reference for each DPLL may be read from the **T(0/4) Auto Active Ref** registers.

The pre-qualification scheme is described in the **Reference Inputs Monitoring and Qualification** section.

Output Clocks

The clock output section includes 8 timing synthesizers and clock drivers. Generates 9 synchronized clocks and T0_XSYNC_OUT. T0 timing generator controls synthesizer G_0~G_6, G_8, and G_9. G_7 is controlled by T4 timing generator as shown in Figure 5.

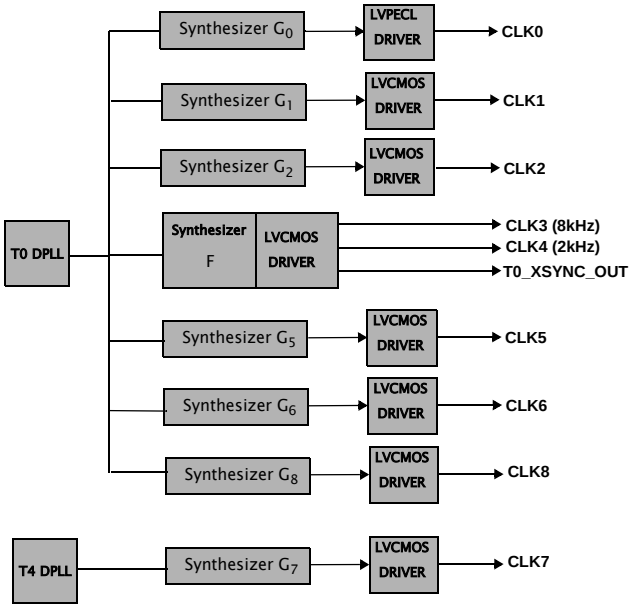


Figure 5: Output Clocks

STC5230-I provides two modes to program the fre-quency of CLK0~CLK8 (except CLK3 and CLK4): Freq Pre Defined mode (default mode) and Freq User Defined mode. CLK3 and CLK4 are frame pulse sig-nal at fixed frequency of 8kHz and 2kHz.

Freq Pre Defined Mode

This mode is enabled for CLK0~CLK8 (except CLK3 and CLK4) individually when associated clock output index is selected at the register **CLK Index Select** and the register **CLK User Defined Freq** is set to 0. In Freq Pre Defined mode, clock outputs of CLK0 ~ CLK8 (except CLK3 and CLK4) are programmable for some certain frequencies at the registers **CLK(0~8) Sel**. This mode is only enabled when value of the register **CLK User Defined Freq** is 0. Each clock of CLK0 ~CLK8 can be put in tri-state by writing 0 to registers **CLK(0~8) Sel** individually. Freq Pre Defined mode is default manner for frequency selection of clock outputs.

In this mode, supported pre-defined frequency of CLK0~CLK8 is shown below:

- **CLK0**: 155.52/125 MHz (LVPECL), selected or put it in tri-state by writing the **CLK0 Sel** register.
- **CLK1**: programmable at 19.44MHz, 38.88MHz, 51.84MHz, 77.76 MHz, 25MHz, 50MHz, 125MHz, and tri-state, by writing to the **CLK1 Sel** register.
- **CLK2**: Programmable at 19.44MHz, 38.88MHz, 51.84, 77.76 MHz, 25MHz, 50MHz, 125MHz and tri-state, by writing to the **CLK2 Sel** register.
- **CLK3**: 8kHz, 50% duty cycle or programmable pulse width, and may be put in tri-state by writing to the **CLK3 Sel** register.
- **CLK4**: 2kHz, 50% duty cycle or programmable pulse width, and may be put in tri-state by writing to the **CLK4 Sel** register.
- **CLK5**: Either DS3 or E3 rate, or “tri-state”, programmed by writing to the **CLK5 Sel** register.
- **CLK6**: Programmable at nxT1 or nxE1 rate, where n=1,2,4,8,16, or may be put in tri-state, by writing to the **CLK6 Sel** register.
- **CLK8**: the second pair of 125 MHz (LVPECL), put in tri-state by writing the **CLK8 Sel** register.
- **CLK7 (T4)**: Either DS1 or E1 rate, or “tri-state”, programmed by writing to the **CLK7 Sel** register.

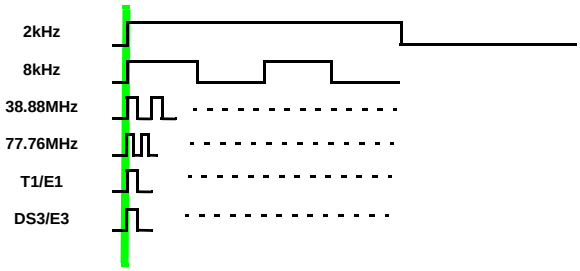


Figure 6: T0 clock output Phase Alignment

In addition, the **T0_XSYNC_OUT** output provides phase information and state data for master/slave operation of the T0 timing generator.

CLK3, 5 and **6** are phase aligned with **CLK4** (2kHz) and 19.44MHz, 38.88MHz, 51.84MHz, 77.76MHz of **CLK1** and **CLK2** are also phase aligned with **CLK4** as shown in Figure 6. 25MHz, 50MHz, 125MHz on **CLK1** is not aligned with **CLK4**. 25MHz, 50MHz, 125MHz on **CLK2** is not aligned with **CLK4** too. **CLK0** and **8** are synchronized to **CLK1~6**, but not phase aligned.

Freq User Defined Mode

Any valid non-zero value of the register **CLK User Defined Freq** enable Freq User Defined mode and output clock at associated frequency based on which clock is selected at the register **CLK Index Select**. In Freq User Defined Mode, the frequency of CLK0~CLK8 (except CLK3 and CLK4) is programmable from 1MHz to 156.25MHz, in 1kHz steps. It supports more flexible choices of frequencies than Freq Pre Defined mode.

In Freq User Defined mode, any of clock outputs (except CLK7 derived from synthesizer G_7 of T4 DPLL) which has frequency at the integer multiple of 8kHz is in phase alignment with the frame pulse output CLK3 (8KHz) if none of clock phase skew is programmed.

Clock Skew Adjustment

The STC5230-I allows user to program the phase skew of each clock output, up and down 50ns in roughly 0.024ns steps. at the register **CLK Skew Adj**. Select clock index at the register **CLK Index Select** to adjust phase skew of associated clock output CLK0~CLK8 and T0_XSYNC_OUT.

Master/Slave Configuration

Pairs of STC5230-I devices may be operated in a mas-ter/slave configuration for added reliability, as shown in Figure 7.

Devices are configured as master/slave pair by cross-connecting their respective **T0_XSYNC_OUT** and/or **T0_XSYNC_IN** pins. The **T0_MS** pins determine the master or slave mode for T0 timing generator: 1=Master, 0=Slave. Thus, master/slave state is always manually controlled by the application. The slave T0 synchronizes and phase-aligns in the 2kHz domain according to data received over the **T0 _XSYNC_OUT/T0_XSYNC_IN** data link from the paired partner.

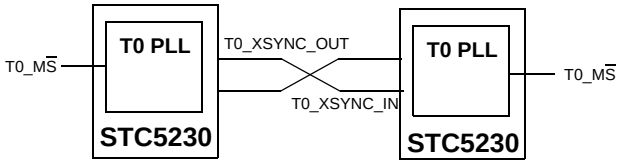


Figure 7: Master/Slave Pair

When two STC5230 are wired in the master/slave pair configuration, the paired T0 timing generators can be running in master/master, master/slave, or slave/master modes. However, both device's timing generators should not be simultaneously operated in the slave mode to avoid the resonance.

The **T0 MS Sts** register reflects the states of the **T0_MS** pin.

Master/Slave Operation

While in the slave configuration, the operation is analogous to the synchronized/master mode. The **T0_XSYNC_OUT** data link/8kHz signals provide the phase information of 2kHz (T0) for phase alignment between the master and the slave. In addition to phase information, **T0_XSYNC_OUT** also provides the reference selection state to ensure that a new master may lock on the same reference if reference selection is in "automatic" mode.

Perfect phase alignment of the **Clk(x)** output clocks (between the paired timing generators in two devices) would require no delay on the cross-coupled data link connection. To accommodate delay on the path, the STC5230 provides a programmable phase compensation feature. See Figure 8. The slave's **Clk(x)** outputs may be phase shifted from 0 to +409.5ns, in 100ps increments according to the contents of the **T0 Slave Phase Adj** registers to compensate for the path delay of the **T0_XSYNC_OUT** to **T0_XSYNC_IN** cross-couple connection. This offset may therefore be programmed to exactly compensate for the actual path delay associated with the particular application's cross-coupled traces. Thus, master/slave switches with the STC5230 devices may be accomplished with near-zero phase hits to the downstream devices.

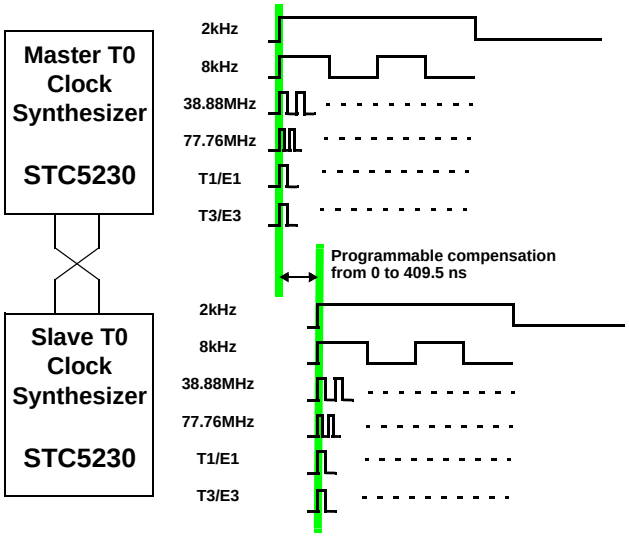


Figure 8: T0 **CLK1-6** Phase Alignment and Master/Slave skew Control

STC5230-I can measure and report the round-trip phase delay of T0's cross-couple links. While T0 is configured in master mode in redundant application, the phase delay between the **T0_XSYNC_OUT** and **T0_XSYNC_IN** pins is continuously measured. The user may read the phase delay from the **T0 MS PHE** register. Advanced users may also use this informa-tion for fault detection purposes.

The first time a timing generator becomes a slave, such as immediately after power-up, its output clock phase starts out arbitrary, and will quickly phase-align to the master unit. The phase error will be eliminated (or converged to the programmed phase offset). The whole pull-in-and-lock process will complete in about 16 seconds. There is no frequency ramp protection in slave mode. Note the phase alignment of all clock outputs from the T0 timing generator with the 2kHz output.

Activity of the signals on the **T0_XSYNC_IN** pin is available in the **Refs Activity** register. (The leaky bucket algorithms are not applied to these signals.)

Once a pair of timing generators has been operating in aligned master/slave mode, and a master/slave switch occurs, the timing generator that becomes master will maintain its output clock phase and frequency while a phase rebuild is performed on its selected reference input. Therefore, as master mode operation commences, there will be no phase or frequency hits on the clock outputs. Assuming the phase offset is programmed for the actual delay of this cross-couple path, there will again be no phase hits on the output clocks of the timing generator that has transitioned from master to slave.

Event Interrupts

The STC5230-I may indicate the occurrence of a num-ber of events as an interrupt to the host processor via pin EVENT_INTR (pin 32). The user may enable or disable individual interrupt by writing to register **Intr Enable**. The associated events which trigged inter-rupts will be latched. After detected the assert of inter-rupt pin, the application may read the list of latched events from register **Intr Event**. The user may clear the events by writing a '1' to the bit position of each related event. The pin **EVENT_INTR** returns to nor-mal when all events are cleared.There are 10 different events that can trigger an inter-rupt. These include any status change of either timing generator and the change of qualification status of input references. The status change of a timing gen-erator includes a change of the active reference in automatic reference selection mode, a change of the DPLL status, and a change of the cross reference activity. Each event may be enabled and disabled individually.

Configuration Data Load and Field Upgradability

Following any device reset, either via power-up or operation of the reset pin, the device needs to be loaded with the configuration data. The loading proce-dure has two stages. First stage is to load core con-figuration data (programmed with factory default). The register **ROM Core Status** may provide the sta-tus of the core configuration data loading process. Second stage is to load hardware and firmware con-figuration data.

This data defines the initialization of registers and DPLL detailed behavior. The hardware and firmware configuration data may be loaded from the internal ROM (programmed by factory), an optional external EEPROM, or from the bus interface. If the load failed, the application must rest the device and repeat the load process. Loading external hard-ware and firmware configuration data via optional external EEPROM or the bus interface may provide the feature of field Upgradability to applications. Hardware and firmware configuration data loading method depends on the configuration pins.

Configuration Pins

The configuration pins LM0 and LM1 determine the hardware and firmware configuration data loading method following a power-up or reset. LM0 and LM1 also allow the application to switch among the controller of ROM, EERPOM and Bus interface in run time. The combination of configuration pins is shown in Table 5.

Note that the configuration pins should not both be high, as device damage may occur.

Table 7: Configuration Pins

LM1	LM0	Description
0	0	ROM mode
0	1	Bus mode
1	0	EEPROM mode
1	1	Reserved - do not use

ROM Mode

When the ROM mode is configured via LM0 and LM1 following a power-up or reset, the hardware and firmware configuration data may be loaded automatically from the internal ROM. The data is programmed by manufacturer. Hardware and firmware configuration data loading via the ROM mode is accomplished using register **ROM Loader Status**. The register provides the status of the core, hardware and firmware configuration data loading process.

Bus Mode

When the Bus Mode is configured via LM0 and LM1 following a power-up or reset, the hardware and firmware configuration data may be loaded from the SPI bus interface using the registers **Bus Loader Status**,

Bus Loader Data, **Bus Loader Counter** and **Bus Core Status**. The hardware and firmware configuration data is provided to the customer per an agreement with the manufacturer. The application shall follow the procedure below:

```
/* --- *
The data array data[10496] contains the hardware/firmware
configuration data, starting from index 0.
 * --- */

Procedure Bus_Load
begin

    Label_Repeat:

    - busy wait until bit "bus ready" in the
      Bus_Loader_Status is equal to '1';
    - for i: = 0 to 10,495 step 1
      begin
        - write data[i] to register Bus_Loader_Data;
        - busy wait until bit "bus ready" in register
          Bus_Loader_Status is equal to '1';
      end

    - if bit "load complete" in register Bus_Loader_Status is
      equal to '0'
      begin
        /* loading failed */
        - reset this device by asserting pin RESET;
        - goto Label_Repeat;
      end

    - if bit "checksum status" in register
      Bus_Loader_Status is equal to '0'
      begin
        /* loading failed */
        - reset this device by asserting pin RESET;
        - goto Label_Repeat;
      end

    /* Bus Loading Success */

end of procedure Bus Load
```

The device will assert the "load complete" bit in register **Bus Loader Status** after the application writes 10,496 bytes into register **Bus Loader Data**.

After the bit "load complete" is asserted, the application shall read and check the bit "checksum status" of register **Bus Load Status**. "1" indicates the checksum passed; "0" indicates a load failure. CRC-16 checksum encryption is used in the hardware/firmware configuration data to assure the detection of transmission error.

Before the "bus ready" bit is asserted or after the "load complete" bit in register **Bus Loader Status** is asserted, all writes to the **Bus Loader Data** register will be ignored.

At any time in the process, the application may read the number of bytes that have been written from the **Bus Loader Counter** register.

The register **Bus Core Status** provides the status of core configuration data loading process.

EEPROM Mode

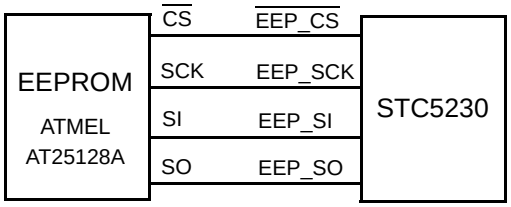
When EEPROM mode is configured via the LM0, LM1 pins, the device may be ready for two processes: hardware and firmware configuration data load process, EEPROM upload and read back process. For the hardware and firmware configuration data load process, the data may be loaded from the optional external EEPROM by the device's built-in EEPROM loader automatically following a power-up or reset. The hardware and firmware configuration data is provided to the customer per an agreement with the manufacturer. Read and check the register **EEP Loader Checksum** which indicates the CRC-16 checksum status of the loading process. The register **EEP Core Status** indicates the checksum status of the core configuration data loading process.
For upload and read back process, the application may read and write the hardware and firmware configuration data from/to the external EEPROM via device's EEPROM controller using the register **EEP Controller Mode**, **EEP Controller Cmd**, **EEP Controller Page**, and **EEP Controller Data**.

After uploading the complete hardware and firmware configuration data to the external EEPROM, the application should read it back and perform the comparison to ensure no transmission errors have happened. The uploading and read back procedures are as follow:

```
Procedure EEP_Upload
begin
    /* --- *
        The data array data[10496] contains the hardware/
        firmware configuration data, starting from index 0.
     * --- */

    - busy wait until bit "ready" in register
      EEP_Controller_Mode is equal to '1';
    - write 0x01 to register EEP_Controller_Mode;
                        /* turn on the write feature */
    - write 0x00 to register EEP_Controller_Cmd;
```

```
                    /* reset the page FIFO buffer */
    - for i = 0 to 163 step 1
      begin
        - write (i) to register EEP_Controller_Page;
                    /* set the page index */
        - for j = 0 to 63 step 1
          begin
            - write data[64*i+j] to register
              EEP_Controller_Data;
          end
        - write 0x01 to register EEP_Controller_Cmd;
                    /* issue the write command */
        - busy wait until bit "ready" in register
          EEP_Controller_Mode is equal to '1';
      end
    - write 0x00 to register EEP_Controller_Mode;
                    /* turn off the write feature */
end of procedure EEP_Write

Procedure EEP_Readback
begin
    - busy wait until bit "ready" in register
      EEP_Controller_Mode is equal to '1';
    - for i = 0 to 163 step 1
      begin
        - write (i) to register EEP_Controller_Page;
                    /* set the page index */
        - write 0x02 to register EEP_Controller_Cmd;
                    /* issue the read command */
        - busy wait until bit "ready" in register
          EEP_Controller_Mode is equal to '1';
        - for j = 0 to 63 step 1
          begin
            - read and copy the value of register
              EEP_Controller_Data into data[64*i+j];
          end
      end

      /* --- *
         The data array data[10496] is then carrying the hard-
         ware/firmware configuration data, starting from index
         0.
       * --- */
end of procedure EEP_Read
```

Table 6 is the recommended list of compatible EEPROM for applications and Figure 9 is the EEPROM interfaces:



Both $\overline{WP}$ and $\overline{HOLD}$ have to be tied high

Figure 9: EEPROM Configuration

Table 8: Compatible EEPROM

Manufacturer	Part Number
ATMEL	AT25128A

Processor Interface Descriptions

The STC5230-I supports the serial SPI bus interface. The description of the SPI bus's interface timing is following:

The SPI interface bus mode uses the $\overline{\text{SPI\_CS}}$, SPI_SCK, SPI_SDI, and SPI_SDO pins, corresponding to CS, SCLK, SDI, and SDO below respectively, with timing as shown in Figure 10 and Figure 11:

Serial Bus Timing

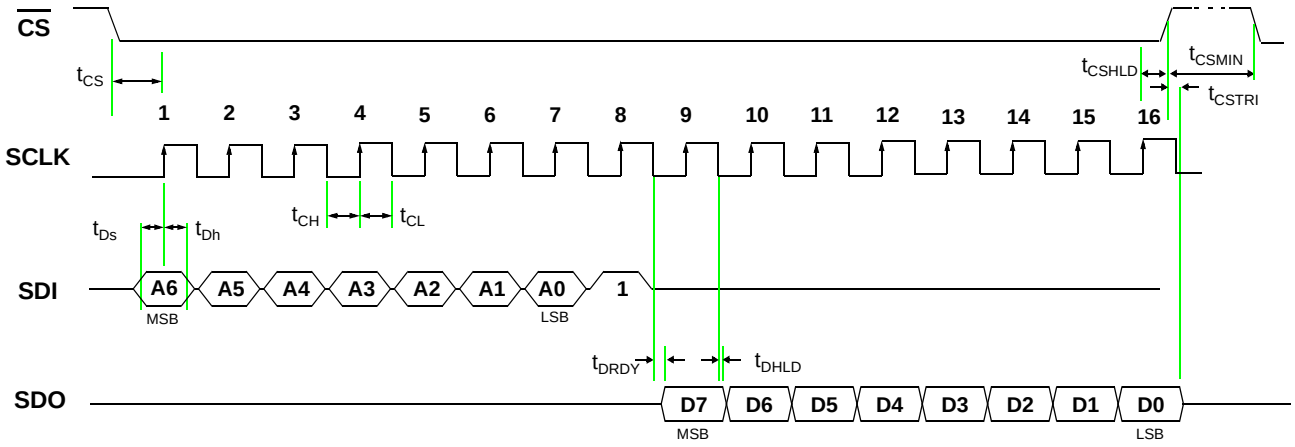


Figure 10: Serial Bus Timing, Read access

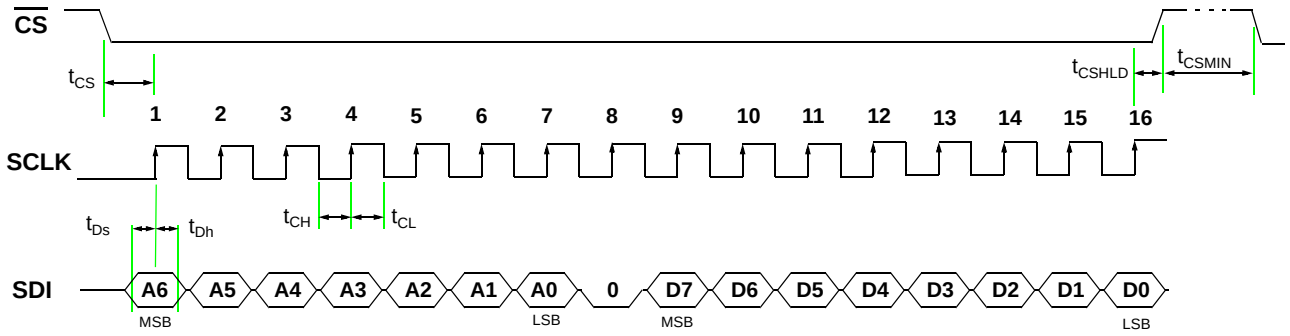


Figure 11: Serial Bus Timing, Write access

Table 9: Serial Bus Timing

Symbol	Description	Min	Max	Unit
t_{CS}	$\overline{CS}$ low to SCLK high	10		ns
t_{CH}	SCLK high time	25		ns
t_{CL}	SCLK low time	25		ns
t_{Ds}	Data setup time	10		ns
t_{Dh}	Data hold time	10		ns
t_{DRDY}	Data ready		7	ns
t_{DHLD}	Data hold	3		ns
t_{CSHLD}	Chip select hold	30		ns
t_{CSTRI}	Chip select to data tri-state		5	ns
t_{CSMIN}	Minimum delay between successive accesses	50		ns

Register Descriptions and Operation

General Register Operation

The STC5230-I device has 1, 2, 3, and 4 byte registers. One-byte registers are read and written directly. Multiple -byte registers must be read and written in a specific manner and order, as follows:

Multibyte register reads

A multibyte register read must commence with a read of the least significant byte first. This triggers a transfer of the remaining byte(s) to a holding register, ensuring that the remaining data will not change with the continuing operation of the device. The remaining byte(s) must be read consecutively with no intervening read/writes from/to other registers.

Multibyte register writes

A multibyte register write must commence with a write to the least significant byte first. Subsequent writes to the remaining byte(s) must be performed in ascending byte order, consecutively, with no intervening read/writes from/to other registers, but with no timing restrictions. Multibyte register writes are temporarily stored in a holding register, and are transferred to the target register when the most significant byte is written.

Clearing bits in the Interrupt Status Register

Interrupt event register **Intr_Event** bits are cleared by writing a “1” to the bit position to be cleared. Interrupt bit positions to be left as is are written with a “0”.

Chip_ID, 0x00 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	0x30							
0x01	0x52							

Indicates chip’s ID number

Chip_Rev, 0x02 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x02	Revision Number							

Indicates the revision number of STC5230. Refer to Order Information for current revision format.

Chip_Sub_Rev, 0x03 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x03	Sub-Revision Number							

Indicates the firmware revision number of STC5230. Refer to Order Information for current revision format.

T0_MS_Sts, 0x04 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x04	Not used							T0 M/S

Reflects the states of the pin T0_$\overline{MS}$. 1 = Master, 0 = slave

T0_Slave_Phase_Adj, 0x05 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x05	Adjust T0 slave phase from 0 ~ 409.5 ns in 0.1 ns steps, lower 8 bits							
0x06	Not used				Adjust T0 slave phase from 0 ~ 409.5 ns in 0.1 ns steps, upper 4 bits			

The T0 slave phase may be adjusted 0 to 409.5 ns relative to the cross couple input with 0.1 ns resolution. This is a 12 bit register, split across address 0x05 and 0x06.

Default value: 0

Fill_Obs_Window, 0x09 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x09	Not used				Leaky bucket fill observation window, *m* = 0 ~ 15			

Sets the fill observation window size for the reference activity monitor to (*m*+1) ms. The window size can be set from 1ms to 16ms.

Default value: *m* = 0, (1ms)

Leak_Obs_Window, 0x0a (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0a	Not used				Leaky bucket leak observation window, *n* = 0 ~ 15			

Sets the leak observation window size for the reference activity monitor to (*n* + 1) times the fill observation window size.

Default value: *n* = 3, (4 times)

Bucket_Size, 0x0b (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0b	Not used		Leaky bucket size, 0 ~ 63					

Sets the leaky bucket size for the reference activity monitor. Bucket size equal to 0 will set the activity monitor off, which will not have the leaky bucket alarm assert or de-assert threshold. Otherwise, the bucket size must be greater than or equal to the alarm assert value. Invalid values will not be written to the register.

Default value: 20

Assert_Threshold, 0x0c (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0c	Not used		Leaky bucket alarm assert threshold, 1 ~ 63					

Sets the leaky bucket alarm assert threshold for the reference activity monitor. The alarm assert threshold value must be greater than the de-assert threshold value and less than or equal to the bucket size value. Invalid values will not be written to the register.

Default value: 15

De_Assert_Threshold, 0x0d (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0d	Not used		Leaky bucket alarm de-assert threshold, 0 ~ 62					

Sets the leaky bucket alarm de-assert threshold for the reference activity monitor. The de-assert threshold value must be less than the assert threshold value. Invalid values will not be written to the register.

Default value: 10

Freerun_Cal, 0x0e (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0e	Lower 8 bits of freerun calibration							
0x0f	Not used					Upper 3 bits of freerun calibration		

Freerun calibration, from -102.4 to +102.3 ppm, in 0.1ppm steps, two's complement.

Default value: 0

Disqualification_Range, 0x10 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x10	Lower 8 bits of disqualification range							
0x11	Not used						Upper 2 bits of disqualification range	

Reference disqualification range, from 0 to +102.3 ppm, in 0.1 ppm steps. This also sets the pull-in range. (See the **Reference Input Monitoring and Qualification** section)

Default value: 110 (range = 11.0 ppm).

Qualification_Range, 0x12 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x12	Lower 8 bits of qualification range							

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x13	Not used						Upper 2 bits of qualification range	

Reference qualification range, from 0 to +102.3 ppm, in 0.1 ppm steps.

Default value: 100 (range = 10.0 ppm).

Qualification_Timer, 0x14 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x14	Not used		0 ~ 63 s					

Reference qualification timer, from 0 to 63 s.

Default value: 10

Ref_Index_Selector, 0x15 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x15	Not used				REF 1 ~ 12			

Determines which of reference inputs is configured individually at the register **Manual_Accept_Ref_Freq** or which of reference has its information read at **Ref_Info**

Valid values from 1 to 12 are relative to Ref1 to Ref12. Invalid values will not be written to the register.

Default value: 1

Ref_Info, 0x16 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x16	Lower 8 bits of frequency offset							
0x17	Reference frequency				Upper 4 bits of frequency offset			

For auto-detect acceptable reference input frequency (Enable at the register **Manual_Accept_Ref_Freq**):

- Indicates the frequency offset and frequency of the reference input selected by the register **Ref_Index_Selector**. Frequency offset is from -204.7 to +204.7 ppm relative to calibrated freerun clock, in 0.1 ppm steps, 2's complement. A value of -2048 indicates the reference is out of range.

For manually acceptable reference input frequency:

- Indicates only the frequency offset of the reference input selected by the register **Ref_Index_Selector**. Field value of Reference frequency (bit7~bit4) will be 15, which means manually acceptable reference input frequency is being used. Refer to the register **Manual_Accept_Ref_Freq** for the manually acceptable frequency setting.

The reference frequency is determined as follows ("Unknown" indicates a signal is present, but frequency is undetermined):

0x17, bits 7 ~ 4	Frequency
0	No signal
1	8 kHz
2	64 kHz
3	1.544 MHz
4	2.048 MHz
5	19.44 MHz
6	38.88 MHz
7	77.76 MHz
8	6.48MHz
9	8.192MHz
10	16.384MHz
11	25 MHz
12	50 MHz
13	125 MHz
14	Unknown
15	Reserved

Refs_Activity, 0x18 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x18	Ref 8	Ref 7	Ref 6	Ref 5	Ref 4	Ref 3	Ref 2	Ref 1
0x19	Not used			T0_XSYNC_IN	Ref 12	Ref 11	Ref 10	Ref 9

Reference activity indicator, 0 = no activity, 1 = activity.

Refs_Qual, 0x1a (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1a	Ref 8	Ref 7	Ref 6	Ref 5	Ref 4	Ref 3	Ref 2	Ref 1
0x1b	Not used				Ref 12	Ref 11	Ref 10	Ref 9

Reference qualification indicator, 0 = not qualified, 1 = qualified.

T0_Control_Mode, 0x1c (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1c	Not used		OOP	Manual/ Auto	Revertive	HO_Usage	Not used	Phase Align Mode

Mode control bits for T0.

Phase Align Mode 0 = Arbitrary, 1 = Align
HO_Usage 0 = Device Holdover History (DHH) is used; 1 = User supplied history is used
Revertive 0 = Non-revertive; 1 = Revertive
Manual/Auto 0 = Manual; 1 = Auto.

OOP In manual mode, when the selected active reference is out of the pull-in range, as specified in register **Disqualification_Range** (0x10). OOP will determine if the reference is to be followed, 0 = Follow, 1 = Don't follow.

Default value: 0

T0_Bandwidth, 0x1d (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1d	Not used			Bandwidth select				

Sets the T0 loop bandwidth:

0x1d, bits 4 ~ 0	Bandwidth, Hz
0	103
1	52
2	27
3	13
4	6.7
5	3.4
6	1.7
7	0.84
8	0.42
9	0.21
10	0.10
31 ~ 11	Reserved

Default value: 6 (1.7Hz)

T0_Auto_Active_Ref, 0x1e (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1e	Not used				Automatically selected active reference for T0			

Indicates the automatically selected active reference for T0, when this T0 is a "master". When this T0 is a "slave", the master's active reference is indicated. (Data valid in automatic mode only)

Bit 3 ~ Bit 0	Selection
0	Freerun
1 ~ 12	Sync with Ref 1 ~ Ref 12
13	Holdover
14, 15	Reserved

T0_Manual_Active_Ref, 0x1f (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1f	Not used				Manual selection of the active reference for T0			

Selects the active reference for T0 in manual reference select mode.

Bit 3 ~ Bit 0	Selection
0	Freerun
1 ~ 12	Sync with Ref 1 ~ Ref 12
13	Holdover
14, 15	Reserved

Default value: 0

T0_Device_Holdover_History, 0x20 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x20	Bits 0 - 7 of 32 bit Device Holdover History							
0x21	Bits 8 - 15 of 32 bit Device Holdover History							
0x22	Bits 16 - 23 of 32 bit Device Holdover History							
0x23	Bits 24 - 31 of 32 bit Device Holdover History							

Device holdover history for T0 relative to MCLK. 2's complement. Resolution is 0.745×10^{-3}ppb.

Default value: 0

T0_Long_Term_Accu_History, 0x24 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x24	Bits 0 - 7 of 32 bit Long Term History							
0x25	Bits 8 - 15 of 32 bit Long Term History							
0x26	Bits 16 - 23 of 32 bit Long Term History							
0x27	Bits 24 - 31 of 32 bit Long Term History							

Long term accumulated history for T0 relative to MCLK. 2's complement. Resolution is 0.745×10^{-3} ppb.

T0_Short_Term_Accu_History, 0x28 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x28	Bits 0 - 7 of 32 bit Short Term History							
0x29	Bits 8 - 15 of 32 bit Short Term History							
0x2a	Bits 16 - 23 of 32 bit Short Term History							
0x2b	Bits 24 - 31 of 32 bit Short Term History							

Short term accumulated history for T0 relative to MCLK. 2's complement. Resolution is 0.745×10^{-3} ppb.

T0_User_Accu_History, 0x2c (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x2c	Bits 0 - 7 of 32 bit User Holdover History							
0x2d	Bits 8 - 15 of 32 bit User Holdover History							
0x2e	Bits 16 - 23 of 32 bit User Holdover History							
0x2f	Bits 24 - 31 of 32 bit User Holdover History							

User accumulated history for T0 relative to MCLK. 2's complement. Resolution is 0.745×10^{-3} ppb.

Default value: 0

T0_History_Ramp, 0x30 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x30	Not used	Long Term History Bandwidth			Short Term History Band-width		Ramp control	

Holdover bandwidth and ramp controls for T0:

0x30, bits 6 ~ 4	Long Term History -3dB Bandwidth
0	4.9 mHz
1	2.5 mHz
2	1.2 mHz
3	0.62 mHz
4	0.31 mHz
5	0.15 mHz
6, 7	Reserved

0x30, bits 3 ~ 2	Short Term History -3dB Bandwidth
0	1.3 Hz
1	0.64 Hz
2	0.32 Hz
3	0.16 Hz

0x30, bits 1 ~ 0	Ramp control
0	No Control
1	1.0 ppm/sec
2	1.5 ppm/sec
3	2.0 ppm/sec

Default value: 0x27 (1.2mHz; 0.64Hz; 2ppm/sec)

T0_Priority_Table, 0x31 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x31	Ref 2 Priority				Ref 1 Priority			
0x32	Ref 4 Priority				Ref 3 Priority			
0x33	Ref 6 Priority				Ref 5 Priority			
0x34	Ref 8 Priority				Ref 7 Priority			
0x35	Ref 10 Priority				Ref 9 Priority			
0x36	Ref 12 Priority				Ref 11 Priority			

Reference priority for automatic reference selection mode. Lower values have higher priority:

0x31 - 0x36, 4 bits	Reference Priority
0	Revoke from auto selection scheme
1 ~ 15	1 ~ 15

Default value: 0

T0_PLL_Status, 0x37 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x37	HHA	AHR	Reserved	SAP	OOP	LOL	LOS	SYNC

SYNC Indicates synchronization has been achieved
0 = Not synchronized
1 = Synchronized

LOS Loss of signal of the active reference
0 = No Loss
1 = Loss

LOL Loss of lock (Failure to achieve or maintain lock)
0 = No loss of lock
1 = Loss of lock

OOP Out of pull-in range
1 = Out of pull-in range
0 = In range

SAP Indicates the output clocks have stopped following the selected reference, caused by out of pull-in range
1 = Stop following at pull-in range boundary
0 = Following

AHR Device Holdover History Tracking
1 = Device holdover history is being tracked
0 = Device holdover history is not tracked, the value based on the latest available history

HHA Indicates if holdover history is available. Config the register **T0_Control_Mode** to select which

of holdover history is used: Device Holdover History or User Supplied History.
1 = Available
0 = Not available

HHA	AHR	Holdover Status
1	1	Holdover History available: Device Holdover History tracking on the current active reference
1	0	Holdover History available: Device Holdover History based on last available history
0	0	Holdover History not available
0	1	Not applicable

T0_Accu_Flush, 0x38 (W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x38	Not used							HO flush

Writing to this register will perform a flush of the accumulated history. Bit HO flush determines which histories are flushed.

HO flush Device Holdover History Tracking
0 = Flush and reset T0 long term history only
1 = Flush/reset both T0 long term history and the T0 device holdover history

T4_Control_Mode, 0x39 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x39	Not used		OOP	Manual/ Auto	Revertive	HO_Usage	Not used	Phase Align

Mode control bits for T4.

Phase Align Mode	0 = Arbitrary, 1 = Align
HO_Usage	0 = Device Holdover History (DHH) is used; 1 = User supplied history is used.
Revertive	0 = Non-revertive; 1 = Revertive.
Manual/Auto	0 = Manual; 1 = Auto.
OOP	In manual mode, when the selected active reference is out of the pull-in range, as specified in register **Disqualification_Range** (0x10). OOP will determine if the reference is to be followed, 0 = Follow, 1 = Don't follow.

Default value: 0

T4_Bandwidth, 0x3a (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x3a	Not used			Bandwidth select				

Sets the T4 loop bandwidth:

0x3a, bits 4 ~ 0	Bandwidth, Hz
0	103
1	52
2	27
3	13
4	6.7
5	3.4
6	1.7
7	0.84
8	0.42
9	0.21
10	0.10
31 ~ 11	Reserved

Default value: 0

T4_Auto_Active_Ref, 0x3b (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x3b	Not used				Automatic selected active reference for T4			

Indicates the automatically selected active reference for T4. (Data valid in automatic mode only)

Bit 3 ~ Bit 0	Selection
0	Freerun
1 ~ 12	Sync with Ref 1 ~ Ref 12
13	Holdover
14, 15	Reserved

T4_Manual_Active_Ref, 0x3c (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x3c	Not used				Manual selection of the active reference for T4			

Selects the active reference for T4 in manual reference select mode.

Bit 3 ~ Bit 0	Selection
0	Freerun
1 ~ 12	Sync with Ref 1 ~ Ref 12
13	Holdover
14	Reserved
15	Lock on T0 output

Default value: 0

T4_Device_Holdover_History, 0x3d (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x3d	Bits 0 - 7 of 32 bit Device Holdover History							
0x3e	Bits 8 - 15 of 32 bit Device Holdover History							
0x3f	Bits 16 - 23 of 32 bit Device Holdover History							
0x40	Bits 24 - 31 of 32 bit Device Holdover History							

Device holdover history for T4 relative to MCLK. 2's complement. Resolution is 0.745×10^{-3}ppb.

Default value: 0

T4_Long_Term_Accu_History, 0x41 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x41	Bits 0 - 7 of 32 bit Long Term History							
0x42	Bits 8 - 15 of 32 bit Long Term History							
0x43	Bits 16 - 23 of 32 bit Long Term History							
0x44	Bits 24 - 31 of 32 bit Long Term History							

Long term accumulated history for T4 relative to MCLK. 2's complement. Resolution is 0.745×10^{-3} ppb.

T4_Short_Term_Accu_History, 0x45 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x45	Bits 0 - 7 of 32 bit Short Term History							
0x46	Bits 8 - 15 of 32 bit Short Term History							
0x47	Bits 16 - 23 of 32 bit Short Term History							
0x48	Bits 24 - 31 of 32 bit Short Term History							

Short term accumulated history for T4 relative to MCLK. 2's complement. Resolution is 0.745×10^{-3} ppb.

T4_User_Accu_History, 0x49 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x49	Bits 0 - 7 of 32 bit User Holdover History							
0x4a	Bits 8 - 15 of 32 bit User Holdover History							
0x4b	Bits 16 - 23 of 32 bit User Holdover History							
0x4c	Bits 24 - 31 of 32 bit User Holdover History							

User accumulated history for T4 relative to MCLK. 2's complement. Resolution is 0.745×10^{-3} ppb.

Default value: 0.

T4_History_Ramp, 0x4d (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x4d	Not used	Long Term History bandwidth			Short Term History bandwidth		Ramp control	

Holdover bandwidth and ramp controls for T4:

0x4d, bits 6 ~ 4	Long Term History -3dB Bandwidth
0	4.9 mHz
1	2.5 mHz
2	1.2 mHz
3	0.62 mHz
4	0.31 mHz
5	0.15 mHz
6, 7	Reserved

0x4d, bits 3 ~ 2	Short Term History -3dB Bandwidth
0	1.3 Hz
1	0.64 Hz
2	0.32 Hz
3	0.16 Hz

0x4d, bits 1 ~ 0	Ramp control
0	No Control
1	1.0 ppm/sec
2	1.5 ppm/sec
3	2.0 ppm/sec

Default value: 0x27 (1.2mHz; 0.64Hz; 2ppm/sec)

T4_Priority_Table, 0x4e (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x4e	Ref 2 Priority				Ref 1 Priority			
0x4f	Ref 4 Priority				Ref 3 Priority			
0x50	Ref 6 Priority				Ref 5 Priority			
0x51	Ref 8 Priority				Ref 7 Priority			
0x52	Ref 10 Priority				Ref 9 Priority			
0x53	Ref 12 Priority				Ref 11 Priority			

Reference priority for automatic reference selection mode. Lower values have higher priority:

0x4e - 0x53, 4 bits	Reference Priority
0	Disable reference

0x4e - 0x53, 4 bits	Reference Priority
1 ~ 15	1 ~ 15

Default value: 0

T4_PLL_Status, 0x54 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x54	HHA	AHR	Reserved	SAP	OOP	LOL	LOS	SYNC

SYNC Indicates synchronization has been achieved
0 = Not synchronized
1 = Synchronized

LOS Loss of signal of the active reference
0 = No Loss
1 = Loss

LOL Loss of lock (Failure to achieve or maintain lock)
0 = No loss of lock
1 = Loss of lock

OOP Out of pull-in range
1 = Out of pull-in range
0 = In range

SAP Indicates the output clocks have stopped following the selected reference, caused by out of pull-in range
1 = Stop following at pull-in range boundary
0 = Following

AHR Device Holdover History Tracking
1 = Device holdover history is being tracked
0 = Device holdover history is not tracked, the value based on the latest available history

HHA Indicates if holdover history is available. Config the register **T4_Control_Mode** to select which of holdover history is used: Device Holdover History or User Supplied History.
1 = Available
0 = Not available

HHA	AHR	Holdover Status
1	1	Holdover History available: Device Holdover History tracking on the current active reference
1	0	Holdover History available: Device Holdover History based on last available history
0	0	Holdover History not available
0	1	Not applicable

T4_Accu_Flush, 0x55 (W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x55	Not used							HO flush

Writing to this register will perform a flush of the accumulated history. The value of bit HO flush determines which histories are flushed.

HO flush Device Holdover History Tracking
0 = Flush and reset T4 long term history only
1 = Flush/reset both T4 long term history and the T4 device holdover history

CLK0_Sel, 0x56 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x56	Not used						CLK0 Select	

Selects frequency of CLK0 or put CLK0 in tri-state in Freq Pre Defined mode. Freq Pre Defined mode (default mode) of CLK0 is enabled by setting the register **CLK_Index_Select** to CLK0 and the register **CLK_User_Defined_Freq** to 0.

0x56, bits 1 ~ 0	CLK0 output
0	Tri-state
1	155.52MHz
2	125MHz
3	Reserved

Default value: 0

CLK1_Sel, 0x57 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x57	Not used					CLK1 Select		

Selects frequency of CLK1 or put CLK1 in tri-state in Freq Pre Defined mode. Freq Pre Defined mode (default mode) of CLK1 is enabled by setting the register **CLK_Index_Select** to CLK1 and the register **CLK_User_Defined_Freq** to 0.

0x57, bits 3 ~ 0	CLK1 output
0	Tri-state
1	19.44MHz
2	38.88MHz
3	77.76MHz
4	51.84MHz
5	25MHz
6	50MHz
7	125MHz

Default value: 1 (19.44MHz)

CLK2_Sel, 0x58 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x58	Not used					CLK2 Select		

Selects frequency of CLK2 or put CLK2 in tri-state in Freq Pre Defined mode. Freq Pre Defined mode (default mode) of CLK2 is enabled by setting the register **CLK_Index_Select** to CLK2 and the register **CLK_User_Defined_Freq** to 0.

0x58, bits 3 ~ 0	CLK2 output
0	Tri-state
1	19.44MHz
2	38.88MHz
3	77.76MHz
4	51.84MHz
5	25MHz
6	50MHz
7	125MHz

Default value: 2 (38.88MHz)

CLK3_Sel, 0x59 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x59	Not used		CLK3 Select					

Selects pulse width of CLK3 (8KHz) or put CLK3 in tri-state. In variable pulse width, the width may be selected from 1 to 62 times the period of the 155.52MHz output (~6.43ns to 399ns).

0x59, bits 5 ~ 0	CLK3 (8kHz) output
0	Tri-state
1 ~ 62	Pulse width 1 to 62 cycles of 155.52MHz
63	50% duty cycle

Default value: 63

CLK4_Sel, 0x5a (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x5a	Not used		CLK4 Select					

Selects pulse width of CLK4 (2kHz) or put CLK4 in tri-state. In variable pulse width, the width may be selected from 1 to 62 times the period of the 155.52MHz output (~6.43ns to 399ns).

0x5a, bits 5 ~ 0	CLK4 (2kHz) output
0	Tri-state
1 ~ 62	Pulse width 1 to 62 cycles of 155.52MHz
63	50% duty cycle

Default value: 63

CLK5_Sel, 0x5b (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x5b	Not used						CLK5 Select	

Selects frequency of CLK2 or put CLK2 in tri-state in Freq Pre Defined mode. Freq Pre Defined mode (default mode) of CLK5 is enabled by setting the register **CLK_Index_Select** to CLK5 and the register **CLK_User_Defined_Freq** to 0.

0x5b, bits 1 ~ 0	CLK5 output
0	Tri-state
1	44.736MHz (DS3)
2	34.368MHz (E3)
3	Reserved

Default value: 2 (44.736MHz)

CLK6_Sel, 0x5c (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x5c	Not used				CLK6 Select			

Selects frequency of CLK6 or put CLK6 in tri-state in Freq Pre Defined mode. Freq Pre Defined mode (default mode) of CLK6 is enabled by setting the register **CLK_Index_Select** to CLK6 and the register **CLK_User_Defined_Freq** to 0.

0x5c, bits 3 ~ 0	CLK6 output
0	Tri-state
1	2.048MHz
2	4.096MHz
3	8.192MHz
4	16.384MHz
5	32.768MHz
6, 7, 8	Reserved
9	1.544MHz
10	3.088MHz
11	6.176MHz
12	12.352MHz
13	24.704MHz
14, 15	Reserved

Default value: 1 (2.048MHz)

CLK7_Sel, 0x5d (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x5d	Not used						CLK7 Select	

Selects frequency of CLK7 (T4) or put CLK7 in tri-state in Freq Pre Defined mode. Freq Pre Defined mode (default mode) of CLK7 is enabled by setting the register **CLK_Index_Select** to CLK7 and the register **CLK_User_Defined_Freq** to 0.

0x5d, bits 1 ~ 0	CLK7 output
0	Tri-state
1	1.544MHz (T1)
2	2.048MHz (E1)
3	Reserved

Default value: 1 (1.544MHz)

Intr_Event, 0x5e (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x5e	Not used		Event 5: T4 DPLL status changed	Event 4: T4 active reference changed in auto selection mode	Event 3: T0 cross reference changed from non-active to active	Event 2: T0 cross reference changed from active to non-active	Event 1: T0 DPLL status changed	Event 0: T0 active reference changed in auto selection mode
0x5f	Not used						Event 9: Any reference changed from disqualified to qualified	Event 8: Any reference changed from qualified to disqualified

Interrupt event, 0 = no event, 1 = event occurred. Interrupt 8 and 9 apply to the 12 reference inputs only. Interrupts are cleared by writing “1’s” to the bit positions to be cleared (See **General Register Operation, Clearing bits in the Interrupt Status Register** section).

Intr_Enable, 0x60 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x60	Not used		Intr 5 Enable	Intr 4 Enable	Intr 3 Enable	Intr 2 Enable	Intr 1 Enable	Intr 0 Enable
0x61	Not used						Intr 9 Enable	Intr 8 Enable

Interrupt disable/enable, 0 = disable, 1 = enable.

Default value: 0

T0_MS_PHE, 0x62 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x62	Bits 0 - 7 of 20 bit Phase Delay							
0x63	Bits 8 - 15 of 20 bit Phase Delay							
0x64	Not used				Bits 16 - 19 of 20 bit Phase Delay			

T0's phase delay of the round-trip cross-couple links from the master to the slave then back to the master. 2's complement. Resolution is (12.5ns/64 ~= 0.2ns). Range from (-125us/2) to (+125us/2). This value is valid only when T0 is configured as in master mode.

CLK8_Sel, 0x65 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x65	Not used						CLK8 Select	

Selects frequency of CLK8 or put CLK8 in tri-state in Freq Pre Defined mode. Freq Pre Defined mode (default mode) of CLK8 is enabled by setting the register **CLK_Index_Select** to CLK8 and the register **CLK_User_Defined_Freq** to 0.

0x65, bits 1 ~ 0	CLK8 output
0	Tri-state
1	125MHz
2	Reserved
3	Reserved

Default value: 0

CLK_Index_Select, 0x66 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x66	Not Used				Clock index selection for clock output frequency in Freq User Defined mode and phase skew adjustment			

Determine which clock output is selected to program frequency in Freq User Defined mode at the register **CLK_User_Defined_Freq** or which clock output is adjusted phase skew at the register **CLK_Skew_Adj**.

Field Value	Clock output
0	CLK0
1	CLK1
2	CLK2
3	Reserved
4	
5	CLK5
6	CLK6

Field Value	Clock output
7	CLK7
8	CLK8
9	CLK3, CLK4, T0_XSYNC_OUT

Default value: 0

CLK_User_Defined_Freq, 0x67 (R/W**)**

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x67	Bits 0-7 of 18 bits Clock Frequency Selection in Freq User Defined mode							
0x68	Bits 15-8 of 18 bits Clock Frequency Selection in Freq User Defined mode							
0x69	Not used						Bits 17-16 of 18 bits Clock Frequency Selection in Freq User Defined mode	

Set to 0 and select associated clock index at the register **CLK_Index_Selector** to enable Freq Pre Defined mode for CLK0~CLK8 individually.

Set to valid non-zero value to enable Freq User Defined mode and program frequency value from 1MHz to 156.25MHz, in 1kHz steps, for CLK0~CLK8 (except CLK3 and CLK4) based on which clock index is selected at register **CLK_Index_Select**. CLK3 and CLK4 has the fixed frequency at 8kHz and 2kHz. Frequency of T0_XSYNC_OUT is fixed as well.

Field Value	CLK frequency
0	Enable Freq Pre Defined mode
1~999	Do Not Use
1000 ~ 156250	1MHz ~ 156.25MHz
156251~262143	Do Not Use

Default value: 0

CLK_Skew_Adj, 0x6a (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x6a	Lower 8 bits of Clock Phase Skew Adjustment							
0x6b	Not used				Higher 4 bits of Clock Phase Skew Adjustment			

Adjust phase skew for CLK0~CLK8 and T0_XSYNC_OUT based on which clock index is selected at the register **CLK_Index_Select**. Phase skew of CLK3, CLK4, and T0_XSYNC_OUT are adjusted simultaneously at this register when T0_XSYNC_OUT is selected at the register **CLK_Index_Select**. The adjustment is from -6400/128 ns to 6396.875/128 ns, which is -50ns ~ 49.976 ns, in 3.125/128 ns steps, 2's complement.

Default value: 0

Manual_Accept_Ref_Freq, 0x6c (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x6c	Lower 8 bits of integer N Select							
0x6d	Not used	Higher 7 bits of integer N Select						

Enable frequency auto detect function or set integer N for the manual acceptable reference frequency for Ref1~Ref12 individually.

Setting this register to 0 to enable the automatic detection for reference input frequency. The auto-detect acceptable reference input frequencies are shown in Table 3.

Select the integer N for the manually acceptable reference at frequency of Nx8kHz (N is integer from 1 to 32767) for REF1 ~ REF12. Which of reference input is selected for the manually acceptable reference is depending on the index selected at the register **Ref_Index_Selector**.

Setting integer N (from 1 to 32767) at this register allows user to manually select the acceptable reference input frequency at the integer multiple of 8kHz, range from 8kHz to 262.136MHz. For instance, user can select integer N = 32000 to manually accept frequency at 32000x8kHz = 256MHz.

Field Value	Integer N Select
0	Enable auto detection for reference input
1~32767	Integer N for the manual acceptable reference frequency

Default value: 0

ROM_Core_Status, 0x75 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x75	Reserved					Hardware and Firmware Configuration Checksum		Core Configuration Checksum

If ROM mode has been selected with pins LM0,1, this register indicates the status of core, hardware and firmware configuration data loading via internal ROM.

Core configuration checksum Set to 1 when the core configuration data loading process is complete and passed.

Hardware and configuration checksum

Bit2	Bit1	Status
0	0	Fail
0	1	Fail
1	0	Fail
1	1	Pass

Bus_Loader_Status, 0x70 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x70	Reserved					load complete	Bus ready	Checksum status

If bus mode has been selected with pins **LM0,1**, this register indicates the loader's status.

Load complete Set to 1 when the loading process is complete in the bus mode.
Bus ready Set to 1 when the device is ready to load data in the bus mode.
Checksum status Set to 1 if the hardware and firmware configuration data load is successful (CRC-16 checksum over the 10,496 bytes of hardware and firmware configuration data passes) in the bus mode. The "checksum status" bit is valid only after the "load complete" bit has been set.

Bus_Loader_Data, 0x71 (W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x71	Data							

If bus mode has been selected with pins **LM0,1**, the hardware and firmware configuration data is written to this register.

Bus_Loader_Counter, 0x72 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x72	Lower 8 bits of bus loader counter							
0x73	Reserved		Higher 6 bits of bus loader counter					

If bus load data mode has been selected with pins **LM0,1**, this register indicates the number of bytes that have been written to the **Bus_Loader_Data** register.

Bus_Core_Status, 0x75 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x75	Reserved							Checksum status

If bus load data mode has been selected with pins **LM0,1**, this register indicates the checksum status of the core configuration data loading process from the bus interface.

Checksum status Set to 1 if the core configuration data loading is successful in the Bus interface mode.

EEP_Loader_Checksum, 0x70 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x70	Reserved							Checksum status

If EEPROM mode has been selected with pins **LM0,1**, this register indicates the checksum status of the hardware and firmware configuration data loading process from the external EEPROM.

Checksum status Set to 1 if the hardware and firmware configuration data load is successful (ensured by the CRC-16 checksum encryption over the 10,496 bytes of hardware and firmware configuration data) in the EEPROM mode.

EEP_Controller_Mode, 0x71 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x71	Ready	Reserved						Writable

If EEPROM mode has been selected with pins **LM0,1**, this register indicates the readiness of the EEPROM controller and can be used to turn on and off the writing feature to the external EEPROM.

ready Set to 1 when the controller's page FIFO buffer is ready to be used for further read and write data from/to the external EEPROM.

writable This bit is used to enable/disable the writing feature to the external EEPROM. Write '1' to this bit makes the EEROM writable. Writing '0' to this bit makes the EEPROM not writable.

EEP_Controller_Cmd, 0x72 (W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x72	Reserved						Command	

If EEPROM mode has been selected with pins **LM0,1**, this register is used to issue the reset, write, and read commands to the EEPROM controller.

0x72, bits 1 ~ 0	Command
0	Reset and clear the page FIFO buffer
1	Trigger the EEPROM controller to write the contents in the 64-byte page FIFO buffer to a page of the external EEPROM
2	Trigger the EEPROM controller to read and copy the 64-byte content of a page of the external EEPROM into the page FIFO buffer
3	Reserved

EEP_Controller_Page, 0x73 (W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x73	Page number							

If EEPROM mode has been selected with pins **LM0,1**, this register is used to specify the index of the page of the EEPROM for the subsequent read or write command. Valid values are from 0 to 163.

EEP_Controller_Data, 0x74 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x74	Data							

If EEPROM mode has been selected with pins **LM0,1**, the data is read and written from/to the page FIFO buffer via this register.

Default value: 0

EEP_Core_Status, 0x75 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x75	Reserved							Checksum status

If EEPROM mode has been selected with pins **LM0,1**, this register indicates the checksum status of the core configuration data loading process from optional external EEPROM.

Checksum status Set to 1 if the core configuration data load is successful in the EEPROM mode.

MCLK_Freq_Reset, 0x7F (R/W)

Register Writes:

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x7F	External oscillator frequency selection							

Select accepted frequency of MCLK input by writing the associated value to this register three times consecutively, with no intervening read/writes from/to other register. The associated values for the four accepted frequency (10MHz, 12.8MHz, 19.2MHz, 20MHz) are as shown in table below. Three times of consecutive writes will trigger internal soft-reset. Initial default accepted frequency for STC5230 is 20MHz. The accepted frequency of MCLK input returns to 20MHz following any regular reset.

Perform writes at least 50us after the regular reset has done.

Associated written values are shown below:

Bit 7 ~ 0	External Oscillator Frequency Selection
0x11	10MHz
0x22	12.8MHz
0x44	19.2MHz
0x88	20MHz

Register Read:

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x7F	FRQID		COUNT		ID_Written_Value			

This register allows the user read back three values as follows:

FRQID
Indicates the ID of the frequency of MCLK that the STC5230-I currently accept. Constant 3 can be read from FRQID initially since the default accepted frequency for the STC5230-I is 20MHz. The value of FRQID can only be updated when three consecutive valid writes are written to the register **MCLK_Freq_Rest** completely.

Bit 7 ~ 6 FRQID	MCLK Frequency
0	10MHz
1	12.8MHz
2	19.2MHz
3	20MHz

COUNT
Indicates how many times this register has been written to. COUNT is set to 1 when each time a different valid associated value is written to for the first time and is clear to 0 after three times valid writes are completed.

As described above in Register Writes, the associated value should be written to this register three times consecutively, with no intervening read/writes from/to other register. If the written value is invalid or the consecutive writes operation is interrupted by reading/writing from/to other register, COUNT is clear to 0.

Bit 5 ~ 4 COUNT	Counter
0	No written or invalid
1	Once
2	Twice
3	Three times

ID_Written_Value
Indicates the ID of associated value that is being written to this register. The ID is updated when each time a different valid associated value is written to this register for the first time.

As described above in Register Writes, the associated value should be written to this register three times consecutively, with no intervening read/writes from/to other register. If the written value is invalid or the consecutive writes operation is interrupted by reading/writing from/to other register, ID_Written_Value is clear to 0.

Bit 3 ~ 0 ID_Written_Value	Written value to this register (0x7F)
0	No written or invalid
1	0x11
2	0x22
4	0x44
8	0x88

Default value: 0xC0 (20MHz)

Noise Transfer Functions

The user may write to T(0/4)_Bandwidth registers to set the loop bandwidth of the DPLL of each timing generator. The noise transfer function of the DPLL filter is determined by the loop bandwidth. Figure 12 shows the noise transfer functions as the loop bandwidths vary from 0.1Hz to 103Hz.

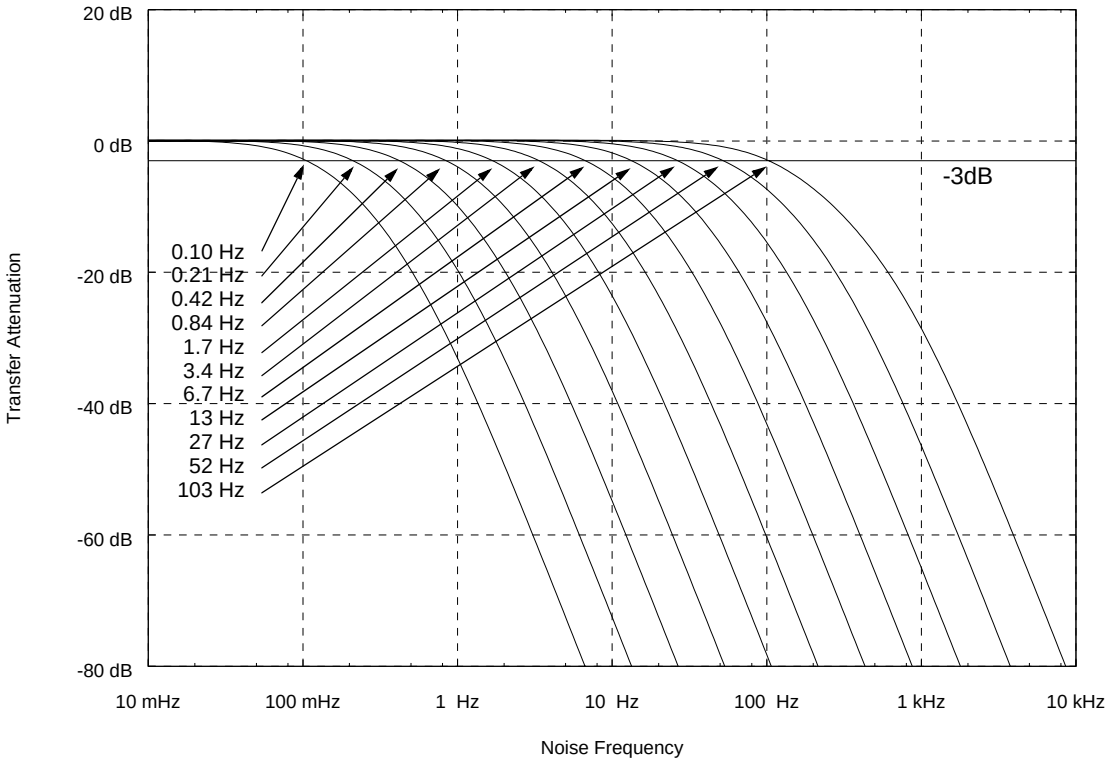


Figure 12: Noise Transfer Functions

Order Information

STC5230-I is RoHS 6/6 compliant.

The product revision number is provided by register **Chip_Rev** (0x02) and **Chip_Sub_Rev** (0x03). The revision number has format of A.B.C. The latest revision number is 3.0.2. It is backward compatible with previous revisions. Distribution of the register address is shown below:

Chip_Rev

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x02	A				B			

Chip_Sub_Rev

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x03	C							

Part Number	Revision Level	Description
STC5230-I	rev 3.0.2	Industrial Temperature Range Model

Specification Modification

This section lists the changes to STC5230 specification from previous revision 2.0.2. Current revision is STC5230-I rev 3.0.2.

- Supports four programmable frequencies of master clock: 10MHz, 12.8MHz, 19.2MHz, and 20MHz. Initial default accepted frequency of MCLK is 20MHz. See Chip Master Clock for details. See register **MCLK_Freq_Reset**.

- Add a function to allow user to program the manually acceptable reference frequency for Ref1~Ref12 individually, at the integer multiple of 8kHz (Nx8kHz, N is integer from 1 to 32767). Some certain SONET and SDH as well as Synchronous Ethernet frequencies (8/64kHz, 1.544/2.048/19.44/38.88/77.76/6.48/8.192/16.384/25/50/125MHz) are auto-detected as in previous revision. See register **Ref_Index_Selector** and **Manual_Accept_Ref_Freq**.

- T4 timing generator does not support slave mode any more. See register **T0_MS_Sts**. Remove pin T4_XSYNC_IN and T4_XSYNC_OUT.

- Remove 1.8V digital/analog power inputs. Supports 3.3V digital power inputs only. Change pin AVdd18, Vdd18, and AVss to NC (connect to ground 0V upto Vdd, or floating)

- Add a function (Freq User Defined mode) to support programming a wide variety of frequencies from 1MHz up to 156.25MHz, in 1kHz steps for CLK0~CLK8 (Except CLK3 and CLK4). See register **CLK_Index_Select** and **CLK_User_Defined_Freq**.

- In Freq Pre Defined mode, frequency 62.5MHz is replaced with 125MHz for CLK1 and CLK2. Low noise 19.44MHz for CLK1 and 15.625MHz for CLK2 are removed. See register **CLK1_Sel** and **CLK2_Sel**.

- Add phase skew adjustment for CLK0~CLK8 and T0_XSYNC_OUT. See register **CLK_Index_Select** and **CLK_Skew_Adj**.

Following table lists the registers are added, removed or changed in revision 3.0.2:

Register Name	Address
Change T0_T4_MS_Sts to T0_MS_Sts	0x04
Remove T4_Slave_Phase_Adj	0x07
Change Ref_Selector to Ref_Index_Selector	0x15
Change Ref_Frq_Offset to Ref_Info	0x16
Disable bit3 of CLK1_Sel	0x57
Disable bit3 of CLK2_Sel	0x58
Add CLK_Index_Select	0x66
Add CLK_User_Defined_Freq	0x67
Add CLK_Skew_Adj	0x6a~0x6b
Add Manual_Accept_Ref_Freq	0x6c~0x6d
Add MCLK_Freq_Reset	0x7F
Remove bit7,6 of register Intr_Event	0x5e
Remove bit7,6 of register Intr_Enable	0x60
Remove bit13 of Refs_Activity	0x18

Application Notes

This section describes typical application use of the STC5230-I device. The General section applies to all appli-cation variations.

General

Power and Ground

Well-planned noise-minimizing power and ground are essential to achieving the best performance of the device. The device requires 3.3 digital power input. All digital I/O is at 3.3V, LVTTL compatible, except for the two pairs of LVPECL clock outputs.

It is desirable to provide individual 0.1uF bypass capacitors, located close to the chip, for each of the power input leads, subject to board space and layout constraints. On power-up, it is desirable to have the 3.3V either lead or be coincident with.

Digital ground should be provided by as continuous a ground plane as possible.

Note: Un-used reference inputs must be grounded.

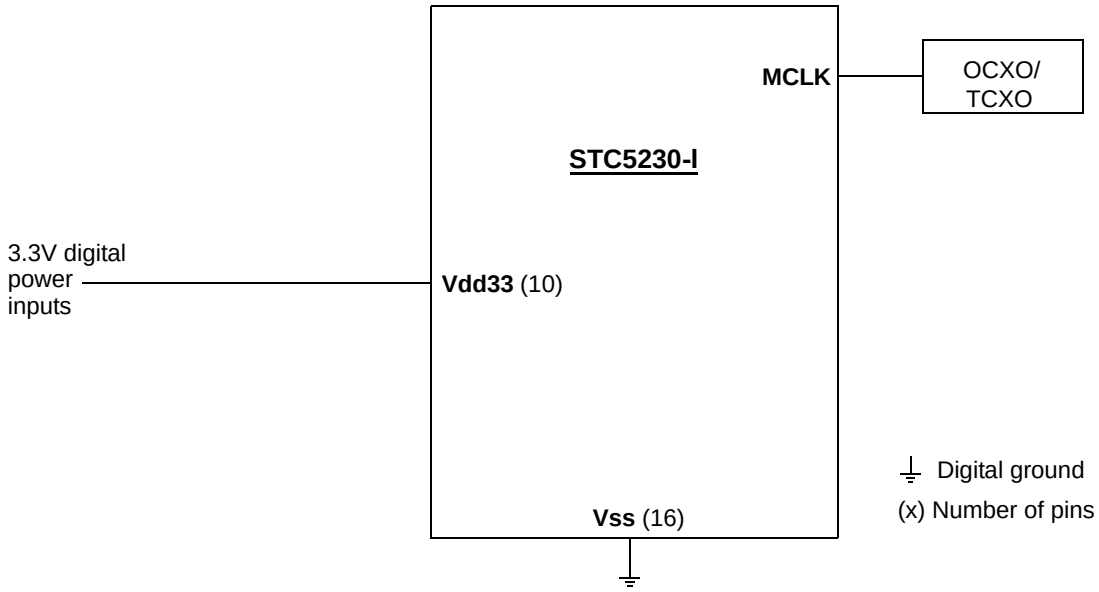
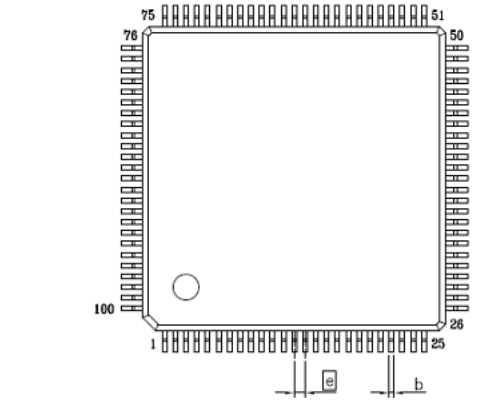
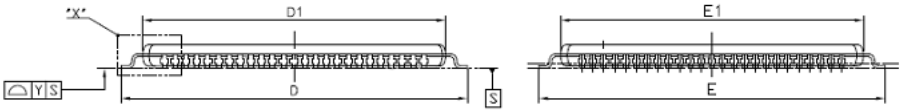


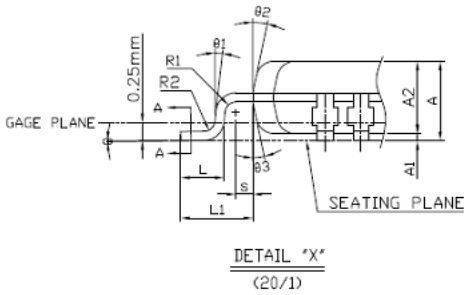
Figure 13: Power and Ground

An external 3.3V LVCMOS level clock (generally derived from TCXO or OCXO) is supplied at pin MCLK as master clock. TCXO or OCXO should be carefully chosen as required by application. It is recommended that the oscillator is placed close to the STC5230-I. Frequency of the master oscillator has four options, see descrip-tion of the register MCLK Freq Reset for details.

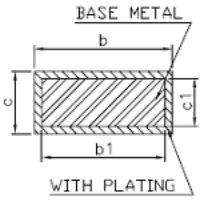
Mechanical Specifications







DETAIL "X"
(20/1)



SECTION A-A

SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			47
A1	0.05		0.15	2		6
A2	0.95	1.00	1.05	37	39	41
b	0.17	0.22	0.27	7	9	11
b1	0.17	0.20	0.23	7	8	9
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D	16.00 BSC			630 BSC		
D1	14.00 BSC			551 BSC		
E	16.00 BSC			630 BSC		
E1	14.00 BSC			551 BSC		
e	0.50 BSC			20 BSC		
L	0.45	0.60	0.75	18	24	30
L1	1.00 REF			39 REF		
R1	0.08			3		
R2	0.08		0.20	3		8
Y			0.075			3
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
s	0.20			8		

NOTES:
1.REFER TO JEDEC MS-026/AED REV. B
2.DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE
MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE
DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED
THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
4.ALL DIMENSIONS IN MILLIMETERS.

Revision History

The following table summarizes significant changes made in each revision. Additions reference current pages.

Revision	Change Description	Pages
P01	Initial issue	
P02	Pin reassignment of CLK0_(P/N) and CLK8_(P/N)	4, 6
	Remove the 155.52MHz output feature from CLK8	1, 6, 10, 17, 40
	Remove the phase align mode feature from Synchronization/Master mode	9, 13, 28, 32
1.0	Add 62.5MHz selection on CLK1 and CLK2	1, 6, 17, 37
	Add maximal value of Tj (operational junction temperature)	7
	Bring back the Phase Align Mode back to Master/Synchronized operational mode	9, 13, 28, 32
	Bring back the Phase Align Mode bit back to register T(0/4)_Control_Mode	9, 13, 28, 32
	Redefine the Phase Align Mode	13
	Change the long term history accumulation filter (order, bandwidth list, and default bandwidth)	14, 30, 34
	Change the short term history accumulation filter (order, bandwidth list, and default bandwidth)	14, 30, 34
	Remove CLK0 from the phase alignment with other clock outputs	18
	Change the loop bandwidth	1, 12, 28, 32, 43
	Change the Transfer Attenuation Function	43
	Change the description of the pull-in process	13
	Remove CLK0 and CLK8 from the title of Figure 8	18
	Correct T3 to DS3 in figure 6	17
	Remove CLK0 and 8 from phase aligned to other T0 clock outputs	18

Revision	Change Description	Pages
P1.1	Change 125MHz of CLK1 to 19.44MHz	6, 10, 17, 37
	Change 125MHz of CLK2 to 15.625MHz	6, 10, 17, 37
	Note 19.44MHz of CLK1 is low noise output	6
	Correct bits range of CLK1_Sel and CLK2_Sel to 3-0	10, 37
	Add description of register 0x75 to register map	10
	Remove the address of registers from detail description.	12, 13, 14, 15, 16, 18, 19
	Change section title of Field Upgradability to Configuration Data Load and Field Upgradability and rewrite the section	19, 20, 21
	Correct R/W of the register T0_T4_MS_Sts to R (read only)	24
	Add description for Revertive and Manual/Auto bit of register 0x1c and 0x39	28, 32
	Add a new section of Specification Modification to note the frequency change for CLK1 and CLK2	46
2.0	Refine register map description	9, 10
	Correct SPI pins name in Processor Interface Descriptions	22
	Correct bits 3-0 description of register Leak_Obs_Window	25
	Refine register detail description of T(0/4)_PLL_Status	32, 37
	Change disable to tri-state for clock outputs	37, 38, 39, 40
	Update section of Specification Modification	47
2.1	Add ITU G.8262 EEC opt1 and opt 2	1

Revision	Change Description	Pages
3.0.2	Add RoHS 6/6 compliant	1, 58
	Add description of supporting four programmable frequencies of external oscillator	1, 13, 15, 17
	Add description of supporting manually acceptable frequency on Ref1~Ref12	1, 14, 15, 20, 21
	Change pin AVdd18, Vdd18, T4_XSYNC_IN, T4_MS, T4_XSYNC_OUT, AVss, AVdd18, and PNC to NC	5, 6, 7
	Change NC pin description	7
	Remove 1.8V digital and analog power input	1, 8, 59
	Replace 62.5MHz with 125MHz on CLK1 and CLK2	6, 10, 19, 22, 43, 44
	Remove low noise 19.44MHz on CLK1 and 15.625MHz on CLK2	6, 10, 19, 22, 43, 44
	Change register name of Ref_Selector to Ref_Index_Selector; Ref_Frq_Offset to Ref_Info;	9, 13, 19, 32,
	Remove register T4_Slave_Phase_Adj	9, 30
	Remove bit13 of register Refs_Activity	9, 33
	Remove bit7,6 of register Intr_Enable and Intr_Event	10, 46
	Remove Bit3 of the register CLK1_Sel and CLK2_Sel	10, 45, 46
	Add register CLK_Index_Select, CLK_User_Defined_Freq, CLK_Skew_Adj, Manual_Accept_Ref_Freq, MCLK_Freq_Reset	11, 49, 50, 51
	Add description of Freq Pre Defined mode and Freq User Defined mode	15, 22, 23
	Modify detail diagram of output clocks Figure 5	22
	Change disable to tristate for CLK0~CLK8	11, 23, 24, 45, 46, 47, 48
	Modify Order Information	57
	Rewrite section of specification modification	58
	Change mechanical specifications due to assembly change	60

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