Precision TCXO
Model DOT702F

CONNOR WINFIELD

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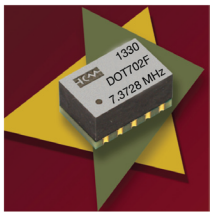
Description:

The Connor-Winfield's DOT702F is a surface mount, 9x14mm, 3.3V, LVCMOS Temperature Compensated Crystal Oscillator (TCXO) designed for applications requiring very tight frequency stability and low phase noise. The RoHS compliant true surface mount package is designed for high-density mounting and is optimum for mass production.



Features:

- 3.3 Vdc Operation
- Frequency Stability: ±0.28 ppm
- Temperature Range: -20 to 70°C
- LVCMOS Output Logic
- 9x14mm SMT Package
- Tape and Reel Packaging
- RoHS Compliant / Pb Free

Absolute Maximum Ratings

Parameter	Minimum	Nominal	Maximum	Units	Notes
Storage Temperature	-55	-	125	°C	
Supply Voltage (Vcc)	-0.5	-	4.5	Vdc	

Absolute Ratings: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only. The functional operation of the device at those or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to conditions outside the "recommended operating conditions" for any extended period of time may adversely impact device reliability and result in failures not covered by warranty.

Operating Specifications

Parameter	Minimum	Nominal	Maximum	Units	Notes
Frequency (Fo)	-	7.3728	-	MHz	
Frequency Calibration @ 25 °C	-1.0	-	1.0	ppm	1
Frequency Stability	-0.28	-	0.28	ppm	2
Aging / Day	-10	-	10	ppb	3
Aging / First Year	-300	-	300	ppb	
Total Frequency Tolerance	-4.6	-	4.6	ppm	4
Frequency vs. Load Stability	-20	-	20	ppb	±5%, 5
Frequency vs. Voltage Stability	-20	-	20	ppb	±5%
Operating Temperature Range:	-20	-	70	°C	
Supply Voltage (Vcc)	3.135	3.3	3.465	Vdc	±5%
Supply Current	-	3	6	mA	
Period Jitter	-	3	5	ps rms	
Integrated Phase Jitter (12 KHz to Fo/2)	-	0.5	1.0	ps rms	
Short Term Stability	-	-	1.0E-9/s		
SSB Phase Noise					
@ 1Hz offset	-	-70	-	dBc/Hz	
@ 10Hz offset	-	-100	-	dBc/Hz	
@ 100Hz offset	-	-130	-	dBc/Hz	
@ 1KHz offset	-	-148	-	dBc/Hz	
@ 10KHz offset	-	-154	-	dBc/Hz	
@ 100KHz offset	-	-155	-	dBc/Hz	
Start-up Time	-	-	10	ms	

RoHS COMPLIANT

Notes:

1. *Frequency referenced to Fo @ 25°C.*
2. *Frequency stability vs. change in temperature. [±(Fmax - Fmin)/(2*Fo)].*
3. *After 30 days of operation.*
4. *Inclusive of calibration @25°C, frequency vs. change in temperature, change in supply voltage(±5%), load change(±5%) and 15 years aging.*
5. *Referenced to 15 pF.*

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LVCMOS Output Characteristics

Parameter	Minimum	Nominal	Maximum	Units	Notes
Load	-	15	-	pF	
Output Voltage					
(High) (Voh)	90% Vcc	-	-	Vdc	
(Low) (Vol)	-	-	10% Vcc	Vdc	
Output Current					
(Ioh)	-	-	4	mA	
(Iol)	-4	-	-	mA	
Duty Cycle at 50% of Vcc	45	50	55	%	
Rise / Fall Time 10% to 90%	-	4	8	ns	

Package Characteristics

Package consisting of a FR4 substrate and a Ryton-R4 cover. Water Resistant, non-hermetic seal

Soldering Characteristics

RoHS compliant lead free. See soldering profile on page 4.

Recommended Cleaning Process

Wash only in an in-line high pressure wash station that has an air knife and drying capabilities.
(Drying temperature range from 85° to 100°C)

Environmental Characteristics

Shock	500 G's 1ms, Half sine, 3 shocks per direction, per MIL- STD 202F, Method 213B Test Condition D.
Sinusoidal Vibration	0.06" D.A. or 10G's Peak, 10 to 500 Hz, per MIL-STD 202F, Method 204D, Test Condition A.
Random Vibration	5.35 G's rms. 20 to 2000 Hz per MIL-STD-202F, Method 214,Test Condition 1A, 15 minutes each axis.
Moisture	10 cycles, 95% RH, Per MIL-STD-202F, Method 112.
Marking Permanency	Per MIL-STD-202F, Method 215J.

Ordering Information

DOT702F - 007.3728M

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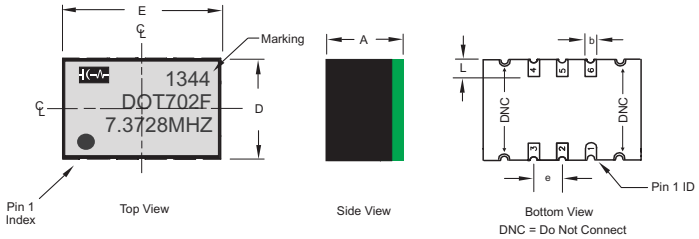
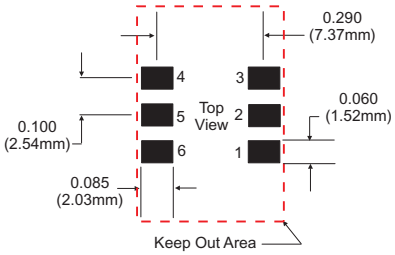
Package Layout



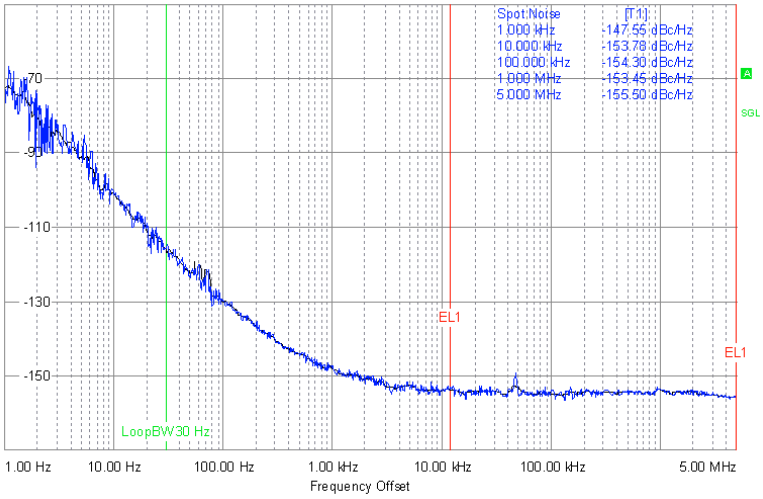
	mm			inches		
Symbol	Min	Nom.	Max.	Min	Nom.	Max.
A	6.60	6.73	6.86	0.260	0.265	0.270
D	8.89	9.02	9.15	0.350	0.355	0.360
E	13.34	13.47	13.60	0.545	0.550	0.555
A1	-	1.58	-	-	0.062	-
L	-	1.52	-	-	0.060	-
b	-	1.02	-	-	0.040	-
e	-	2.54	-	-	0.100	-

Suggested Pad Layout



Keep Out Area Note: Do not route any traces under the device in the keep out area.

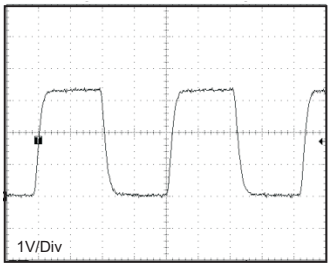
Phase Noise Plot



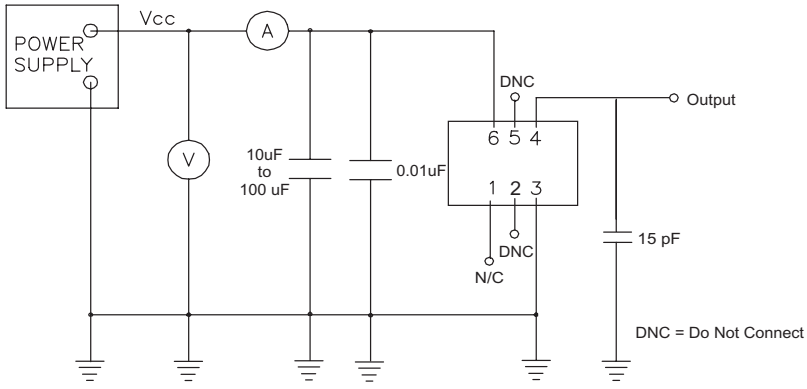
Pad Connections

1:	**N/C**
2:	**Do Not Connect**
3:	**Ground**
4:	**Output**
5:	**Do Not Connect**
6:	**Supply Voltage (Vcc)**

Output Waveform



Test Circuit



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Date	06 May 2019

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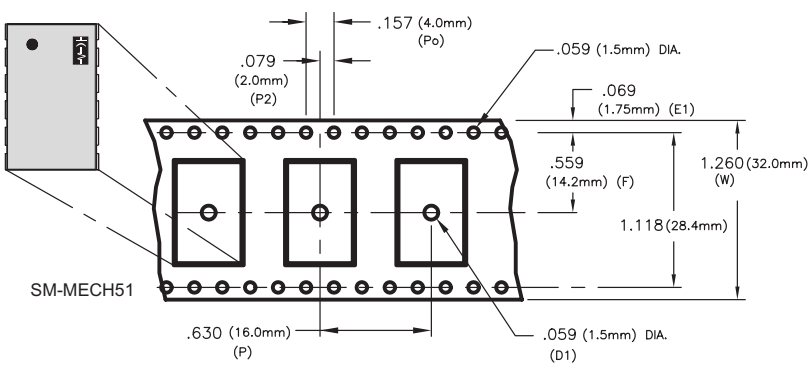
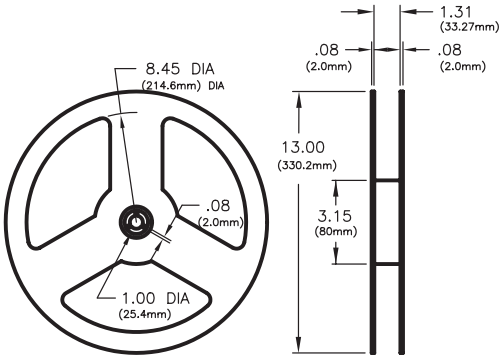
Tape and Reel Dimensions

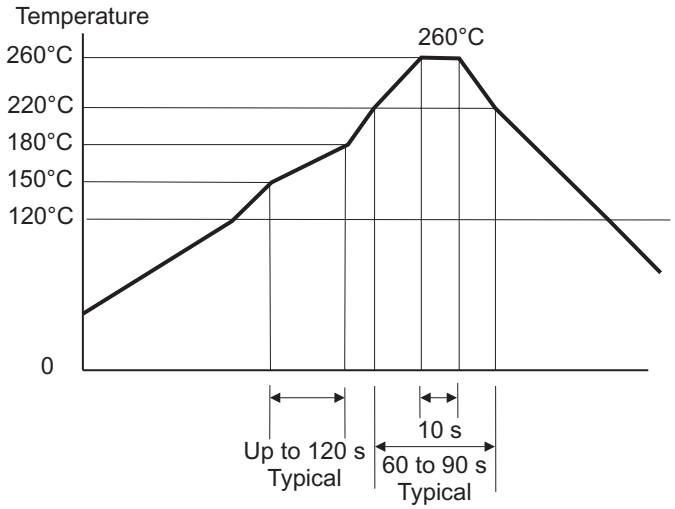
MEETS EIA-481A & EIAJ-1009B
500 PCS/REEL MAXIMUM

DIRECTION OF FEED (CUSTOMER)





Solder Profile



Meets IPC/JEDEC J-STD-020C

Revision History

Revision	Date	Description
00	09/25/14	Data sheet released.
01	05/06/19	Updated Tape and Reel Specifications