CONNOR WINFIELD

NEWS RELEASE

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Connor-Winfield's New STC5230 is a Single Chip Synchronous Clock Solution for SETS

Aurora, IL – The STC5230 is a single chip solution of timing source in SDH, SONET, and Synchronous Ethernet network elements. The device is fully compliant with ITU-G.813 and Telcordia GR1244 and GR253.

The STC5230 accepts 12 reference inputs and generates 9 independent synchronized output clocks. Reference input frequencies are automatically detected, and inputs are individually monitored for quality. Active reference selection may be manual or automatic. All reference switches are hitless. Synchronized outputs may be programmed for a wide variety of SONET and SDH as well as Synchronous Ethernet frequencies.

Two independent timing generators, T0 and T4, provide the essential functions for Synchronous Equipment Timing Source (SETS). Each timing generator includes a DPLL (Digital Phase-Locked Loop), which may operate in the Freerun, Synchronized, and Holdover modes. Both timing generators support master/slave operation for redundant applications. The proprietary SyncLink™ cross-couple data link provides master/slave phase information and state data to ensure seamless side switches.

A standard SPI serial bus interface provides access to the STC5230's comprehensive, yet simple to use internal control and status registers. The device operates with an external OCXO or TCXO as its MCLK at 20 MHz.

The STC5230 is capable of field upgrade with optional external EEPROM or via the bus interface.

Product Features:

- For SDH SETS, SONET Stratum 3, 4E, 4 and SMC, and Synchronous Ethernet
- Two timing generators, T0 and T4, for SETS
- Complies with ITU-G.813, Telcordia GR1244, and GR253
- Supports Master/Slave redundant application with the SyncLink™ cross-couple data links
- Accepts 12 individual clock reference inputs
- Reference clock inputs are automatically frequency detected; each is monitored for quality
- Supports manual and automatic reference selection
- T0 and T4 have independent reference lists and priority tables for automatic reference selection
- Output 9 synchronized clocks
- Could compensate the phase delay of the cross-couple links, in 0.1ns steps up to 409.5ns
- Capable to trace the round-trip phase delay of the master/slave cross-couple links
- Hit-less reference and master/slave switching
- Phase rebuild on re-lock and reference switches
- Programmable loop bandwidth of each DPLL of the T0 and T4 timing generator, from 90 mHz to 107Hz
- Supports SPI bus interface
- Field upgrade capability
- IEEE 1149.1 JTAG boundary scan
- Available in TQ100 package

Price: $40.00

For more information contact:
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