CONNOR WINFIELD

NEWS RELEASE

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Connor-Winfield Announces New STC5420 Series of Timing Chips for SDH/SETS, SONET and Synchronous Ethernet

Aurora, IL – The RoHS 6/6 compliant STC5420 Series are single chip clock synchronization solutions for applications in SDH/SETS, SONET and Synchronous Ethernet network elements. The devices are fully compliant with ITU-T G.813 option 1 and 2 and Telcordia GR1244 and GR253.

The STC5420 Series accepts 12 clock reference inputs from 8kHz to 125 MHz in LVPECL, LVCMOS or LVDS and generates 10 synchronized clock outputs from 2kHz to 312.5 MHz in LVCMOS, LVPECL or LVDS. The synchronized outputs may be programmed for wide variety of frequencies including Nx8kHz, OC-n, Ethernet frequencies and framing pulse clocks. Reference inputs are individually monitored for activity and quality. Reference selection may be manual, fast-manual or automatic.

Independent timing generators operate in Freerun, Synchronized, Pseudo-holdover and Holdover mode. Each timing generator includes a DSP-based PLL. SDP-based PLL technology removes the need for any external parts except the 12.8 MHz oscillator and provides excellent performance and reliability for the STC5420 Series models.

Additionally, within the STC5420 product line, a smaller TQ64 package configuration option is available (p/n STC5425) as well as part number configurations that allow for reduced functionality and lower cost. Please contact us for details.

Features
- Supports Master/Slave and Multiple Master redundant applications
- 7 clock synthesizers generate frequencies: 1xOC-N, x1 Ethernet, x4 general purpose, x1 framing pulse.
- Provides programmable compensation for phase delay between master and slave unit in 0.1 ns steps
- Phase align or hitless reference locking/switching
- Programmable loop bandwidth from 0.1 Hz to 100 Hz
- Programmable phase skew in synthesizer level
- Supports bus interface: Intel, Motorola, Multiplex, SPI
- Single 3.3 V operation
- IEEE 1149.1 JTAG boundary scan

Pricing: $35 at 1K

For more information contact:
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